TL07xx Low-Noise JFET-Input Operational Amplifiers

1 Features

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion: 0.003% (Typical)
- Low Noise
  V_n = 18 nV/$\sqrt{\text{Hz}}$ (Typical) at f = 1 kHz
- High-Input Impedance: JFET Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate: 13 V/μs (Typical)
- Common-Mode Input Voltage Range Includes V_{CC+}

2 Applications

- Motor Integrated Systems: UPS
- Drives and Control Solutions: AC Inverter and VF Drives
- Renewables: Solar Inverters
- Pro Audio Mixers
- DLP Front Projection System
- Oscilloscopes

3 Description

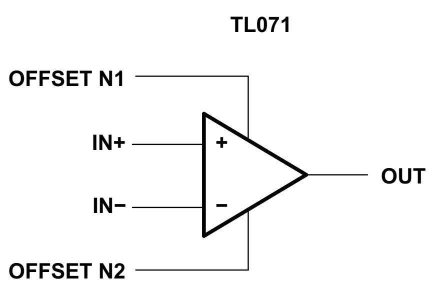
The TL07xx JFET-input operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low-input bias and offset currents, and low offset-voltage temperature coefficient. The low harmonic distortion and low noise make the TL07x series ideally suited for high-fidelity and audio pre-amplifier applications. The TL071 device has offset pins to support external input offset correction.

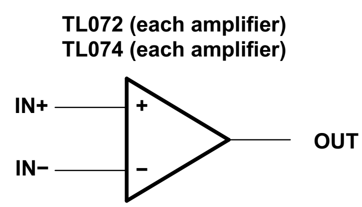
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL07xxD	SOIC (14)	8.65 mm × 3.91 mm
	SOIC (8)	4.90 mm x 3.90 mm
TL07xxJG	CDIP (8)	9.59 mm x 6.67 mm
TL074xJ	CDIP (14)	19.56 mm × 6.92 mm
TL07xxP	PDIP (8)	9.59 mm x 6.35 mm
TL07xxPS	SO (8)	6.20 mm x 5.30 mm
TL074xN	PDIP (14)	19.3 mm × 6.35 mm
TL074xNS	SO (14)	10.30 mm × 5.30 mm
TL07xxPW	TSSOP (8)	4.40 mm x 3.00 mm
TL074xPW	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Symbols





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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (February 2014) to Revision N — **Page**

- Updated data sheet text to latest documentation and translation standards ... 1
- Added TL072M and TL074M devices to data sheet ... 1
- Rewrote text in *Description* section ... 1
- Changed TL07x 8-pin PDIP package to 8-pin CDIP package in *Device Information* table ... 1
- Deleted 20-pin LCCC package from *Device Information* table ... 1
- Added 2017 copyright statement to front page schematic ... 1
- Deleted TL071x FK (LCCC) pinout drawing and pinout table in *Pin Configurations and Functions* section ... 4
- Updated pinout diagrams and pinout tables in *Pin Configurations and Functions* section ... 5
- Deleted differential input voltage parameter from *Absolute Maximum Ratings* table ... 10
- Deleted table notes from *Absolute Maximum Ratings* table ... 10
- Added new table note to *Absolute Maximum Ratings* table ... 10
- Changed minimum supply voltage value from –18 V to –0.3 V in *Absolute Maximum Ratings* table ... 10
- Changed maximum supply voltage from 18 V to 36 V in *Absolute Maximum Ratings* table ... 10
- Changed minimum input voltage value from –15 V to V_{CC-} – 0.3 V in *Absolute Maximum Ratings* table ... 10
- Changed maximum input voltage from 15 V to V_{CC-} + 36 V in *Absolute Maximum Ratings* table ... 10
- Added input clamp current parameter to *Absolute Maximum Ratings* table ... 10
- Changed common-mode voltage maximum value from V_{CC+} – 4 V to V_{CC+} in the *Recommended Operating Conditions* table ... 10

Revision History (continued)

- Changed devices in *Recommended Operating Conditions* table from TL07xA and TL07xB to TL07xAC and TL07xBC 10
- Added TL07xI operating free-air temperature minimum value of –40°C to *Recommended Operating Conditions* table ... 10
- Added U (CFP) package thermal values to *Thermal Information: TL072x (cont.)* table 11
- Added W (CFP) package thermal values to *Thermal Information: TL074x (cont.)* table 12
- Added Figure 20 to Table 1 20
- Added Figure 20 to *Typical Characteristics* section 24
- Added second *Typical Application* section application curves 29
- Reformatted document references in *Layout Guidelines* section 32
- Updated formatting of document reference in *Related Documentation* section 34

Changes from Revision L (February 2014) to Revision M	Page

- Added *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section 1
- Moved *Typical Characteristics* into *Specifications* section. 20

Changes from Revision K (January 2014) to Revision L	Page

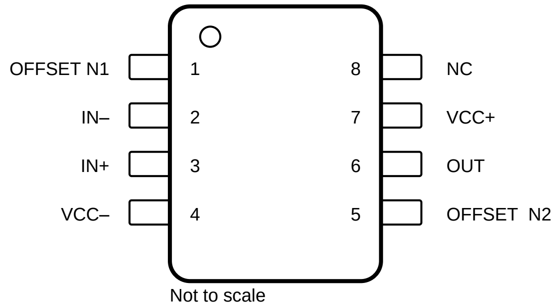
- Moved T_{stg} to *Handling Ratings* table 10
- Added *Device and Documentation Support* section 34
- Added *Mechanical, Packaging, and Orderable Information* section 34

Changes from Revision J (March 2005) to Revision K	Page

- Updated document to new TI datasheet format - no specification changes. 1
- Added ESD warning 34

5 Pin Configuration and Functions

TL071x D, P, and PS Package
8-Pin SOIC, PDIP, SO
Top View

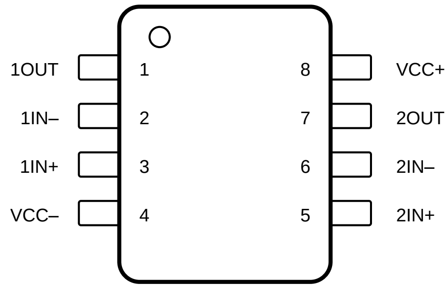


NC- no internal connection

Pin Functions: TL071x

PIN		I/O	DESCRIPTION
NAME	NO.		
IN–	2	I	Inverting input
IN+	3	I	Noninverting input
NC	8	—	Do not connect
OFFSET N1	1	—	Input offset adjustment
OFFSET N2	5	—	Input offset adjustment
OUT	6	O	Output
VCC–	4	—	Power supply
VCC+	7	—	Power supply

TL072x D, JG, P, PS and PW Package
8-Pin SOIC, CDIP, PDIP, SO
Top View

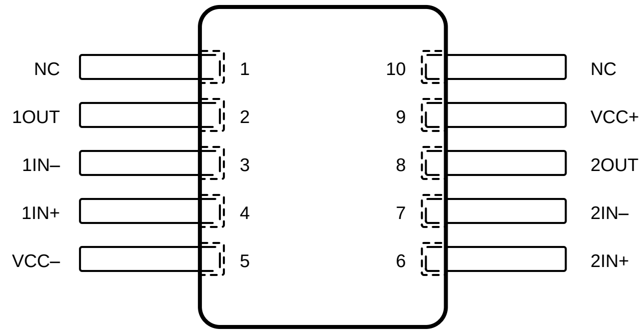


Not to scale

Pin Functions: TL072x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Inverting input
1IN+	3	I	Noninverting input
1OUT	1	O	Output
2IN–	6	I	Inverting input
2IN+	5	I	Noninverting input
2OUT	7	O	Output
VCC–	4	—	Power supply
VCC+	8	—	Power supply

TL072x U Package
10-Pin CFP
Top View



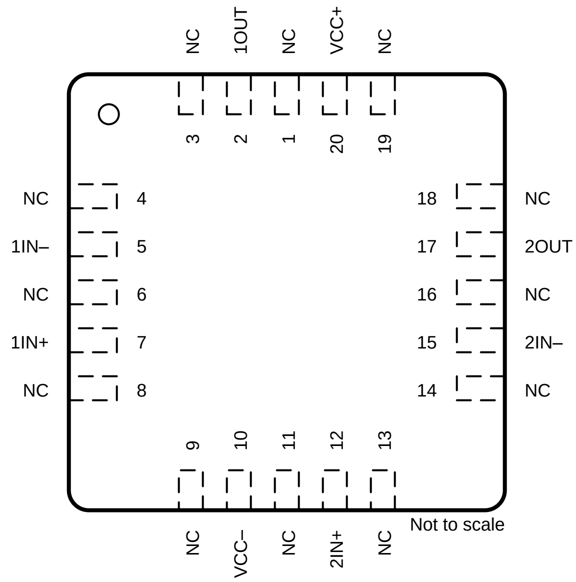
Not to scale

NC- no internal connection

Pin Functions: TL072x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	3	I	Inverting input
1IN+	4	I	Noninverting input
1OUT	2	O	Output
2IN–	7	I	Inverting input
2IN+	6	I	Noninverting input
2OUT	8	O	Output
NC	1, 10	—	Do not connect
VCC–	5	—	Power supply
VCC+	9	—	Power supply

TL072 FK Package
20-Pin LCCC
Top View

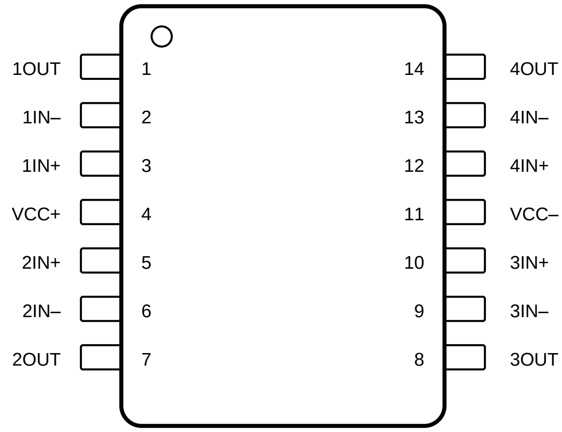


NC- no internal connection

Pin Functions: TL072x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	5	I	Inverting input
1IN+	7	I	Noninverting input
1OUT	2	O	Output
2IN–	15	I	Inverting input
2IN+	12	I	Noninverting input
2OUT	17	O	Output
NC	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	Do not connect
VCC–	10	—	Power supply
VCC+	20	—	Power supply

TL074 D, N, NS, PW, J, and W Packages
14-Pin SOIC, PDIP, SO, TSSOP, CDIP and CFP
Top View



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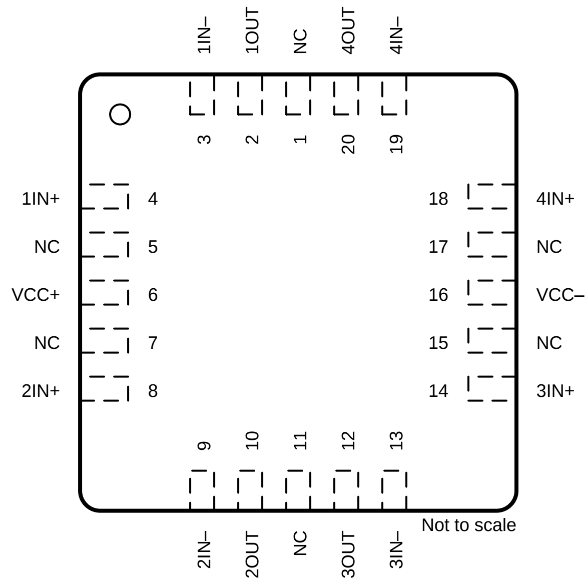
Pin Functions: TL074x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Inverting input
1IN+	3	I	Noninverting input
1OUT	1	O	Output
2IN–	6	I	Inverting input
2IN+	5	I	Noninverting input
2OUT	7	O	Output
3IN–	9	I	Inverting input
3IN+	10	I	Noninverting input
3OUT	8	O	Output
4IN–	13	I	Inverting input
4IN+	12	I	Noninverting input
4OUT	14	O	Output
V_{CC-}	11	—	Power supply
V_{CC+}	4	—	Power supply

TL074 FK Package
20-Pin LCCC
Top View



NC- no internal connection

Pin Functions: TL074x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	3	I	Inverting input
1IN+	4	I	Noninverting input
1OUT	2	O	Output
2IN–	9	I	Inverting input
2IN+	8	I	Noninverting input
2OUT	10	O	Output
3IN–	13	I	Inverting input
3IN+	14	I	Noninverting input
3OUT	12	O	Output
4IN–	19	I	Inverting input
4IN+	18	I	Noninverting input
4OUT	20	O	Output
NC	1, 5, 7, 11, 15, 17	—	Do not connect
VCC–	16	—	Power supply
VCC+	6	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
V_{CC+} - V_{CC-}	Supply voltage	–0.3	36	V
V_I	Input voltage [2]	V_{CC-} – 0.3	V_{CC-} + 36	V
I_{IK}	Input clamp current		–50	mA
	Duration of output short circuit [3]	Unlimited		
T_J	Operating virtual junction temperature		150	°C
	Case temperature for 60 seconds - FK package		260	°C
	Lead temperature 1.8 mm (1/16 inch) from case for 10 seconds		300	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Differential voltage only limited by input voltage.
(3) The output may be shorted to ground or to either supply. Temperature and supply voltages must be limited to ensure that the dissipation rating is not exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage [1]		5	15	V
V_{CC-}	Supply voltage [1]		–5	–15	V
V_{CM}	Common-mode voltage		V_{CC-} + 4	V_{CC+}	V
T_A	Operating free-air temperature	TL07xM	–55	125	°C
		TL08xQ	–40	125	
		TL07xI	–40	85	
		TL07xAC, TL07xBC, TL07xC	0	70	

(1) V_{CC+} and V_{CC-} are not required to be of equal magnitude, provided that the total V_{CC} (V_{CC+} – V_{CC-}) is between 10 V and 30 V.

6.4 Thermal Information: TL071x

THERMAL METRIC(1)		TL071x D (SOIC) 8 PINS	TL071x P (PDIP) 8 PINS	TL071x PS (SO) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	85	95	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: TL072x

THERMAL METRIC(1)		TL072x D (SOIC) 8 PINS	TL072x JG (CDIP) 8 PINS	TL072x P (PDIP) 8 PINS	TL072x PS (SO) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	—	85	95	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	15.05	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: TL072x (cont.)

THERMAL METRIC(1)		TL072x PW (TSSOP) 8 PINS	TL072x U (CFP) 10 PINS	TL072x FK (LCCC) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	169.8	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	62.1	5.61	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	—	176.2	—	°C/W
ψ_{JT}	Junction-to-top characterization parameter	—	48.4	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	—	144.1	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	5.4	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Thermal Information: TL074x

THERMAL METRIC(1)		TL074x D (SOIC) 14 PINS	TL074x N (PDIP) 14 PINS	TL074x NS (SO) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86	80	76	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.8 Thermal Information: TL074x (cont).

THERMAL METRIC[1]		TL074x			UNIT
		J (CDIP)	PW (TSSOP)	W (CFP)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	—	113	128.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.5	—	56.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	—	—	127.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	—	—	29	°C/W
ψ_{JB}	Junction-to-board characterization parameter	—	—	106.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.9 Thermal Information: TL074x (cont).

THERMAL METRIC[1]		TL074x	UNIT
		FK (LCCC)	
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.61	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.10 Electrical Characteristics: TL071C, TL072C, TL074C

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1) (2)		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		3	10	mV
			T_A = Full range			13	
α	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	T_A = Full range		18		µV/°C
I_{IO}	Input offset current	V_O = 0	T_A = 25°C		5	100	pA
			T_A = Full range			10	nA
I_{IB}	Input bias current (3)	V_O = 0	T_A = 25°C		65	200	pA
			T_A = Full range			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L= 10 kΩ	T_A = 25°C	±12	±13.5		V
		R_L≥ 10 kΩ	T_A = Full range	±12			
		R_L≥ 2 kΩ		±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L≥ 2 kΩ	T_A = 25°C	25	200		V/mV
			T_A = Full range	15			
B_1	Utility-gain bandwidth	T_A = 25°C			3		MHz
r_I	Input resistance	T_A = 25°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = $V_{ICR(min)}$, V_O = 0, R_S = 50 Ω	T_A = 25°C	70	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	T_A = 25°C	70	100		dB
I_{CC}	Supply current (each amplifier)	V_O = 0; no load	T_A = 25°C		1.4	2.5	mA
V_{O1} / V_{O2}	Crosstalk attenuation	A_{VD} = 100	T_A = 25°C		120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
(2) Full range is T_A = 0°C to 70°C.
(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 1. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

6.11 Electrical Characteristics: TL071AC, TL072AC, TL074AC

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS [1] [2]		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0 R_S = 50 Ω	T_A = 25°C		3	6	mV
			T_A = Full range			7.5	
α	Temperature coefficient of input offset voltage	V_O = 0 R_S = 50 Ω	T_A = Full range		18		μV/°C
I_{IO}	Input offset current	V_O = 0	T_A = 25°C		5	100	pA
			T_A = Full range			2	nA
I_{IB}	Input bias current [3]	V_O = 0	T_A = 25°C		65	200	pA
			T_A = Full range			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L= 10 kΩ	T_A = 25°C	±12	±13.5		V
		R_L≥ 10 kΩ	T_A = Full range	±12			
		R_L≥ 2 kΩ		±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V R_L≥ 2 kΩ	T_A = 25°C	50	200		V/mV
			T_A = Full range	25			
B_1	Utility-gain bandwidth	T_A = 25°C			3		MHz
r_I	Input resistance	T_A = 25°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = $V_{ICR(min)}$ V_O = 0 R_S = 50 Ω	T_A = 25°C	75	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	V_{CC} = ±9 V to ±15 V V_O = 0 R_S = 50 Ω	T_A = 25°C	80	100		dB
I_{CC}	Supply current (each amplifier)	V_O = 0; no load	T_A = 25°C		1.4	2.5	mA
V_{O1} / V_{O2}	Crosstalk attenuation	A_{VD} = 100	T_A = 25°C		120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
(2) Full range is T_A = 0°C to 70°C.
(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 1. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

6.12 Electrical Characteristics: TL071BC, TL072BC, TL074BC

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1) (2)		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		2	3	mV
			T_A = Full range			5	
α	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	T_A = Full range		18		μV/°C
I_{IO}	Input offset current	V_O = 0	T_A = 25°C		5	100	pA
			T_A = Full range			2	nA
I_{IB}	Input bias current (3)	V_O = 0	T_A = 25°C		65	200	pA
			T_A = Full range			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	T_A = 25°C	±12	±13.5		V
		R_L ≥ 10 kΩ	T_A = Full range	±12			
		R_L ≥ 2 kΩ		±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	T_A = 25°C	50	200		V/mV
			T_A = Full range	25			
B_1	Utility-gain bandwidth	T_A = 25°C			3		MHz
r_I	Input resistance	T_A = 25°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = $V_{ICR(min)}$, V_O = 0, R_S = 50 Ω	T_A = 25°C	75	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	T_A = 25°C	80	100		dB
I_{CC}	Supply current (each amplifier)	V_O = 0; no load	T_A = 25°C		1.4	2.5	mA
V_{O1} / V_{O2}	Crosstalk attenuation	A_{VD} = 100	T_A = 25°C		120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
(2) Full range is T_A = 0°C to 70°C.
(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 1. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

6.13 Electrical Characteristics: TL071I, TL072I, TL074I

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1) (2)		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0 R_S = 50 Ω	T_A = 25°C		3	6	mV
			T_A = Full range			8	
α	Temperature coefficient of input offset voltage	V_O = 0 R_S = 50 Ω	T_A = Full range		18		μV/°C
I_{IO}	Input offset current	V_O = 0	T_A = 25°C		5	100	pA
			T_A = Full range			2	nA
I_{IB}	Input bias current (3)	V_O = 0	T_A = 25°C		65	200	pA
			T_A = Full range			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L= 10 kΩ	T_A = 25°C	±12	±13.5		V
		R_L ≥ 10 kΩ	T_A = Full range	±12			
		R_L ≥ 2 kΩ		±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V R_L ≥ 2 kΩ	T_A = 25°C	50	200		V/mV
			T_A = Full range	25			
B_1	Utility-gain bandwidth	T_A = 25°C			3		MHz
r_I	Input resistance	T_A = 25°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = $V_{ICR(min)}$ V_O = 0 R_S = 50 Ω	T_A = 25°C	75	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V V_O = 0 R_S = 50 Ω	T_A = 25°C	80	100		dB
I_{CC}	Supply current (each amplifier)	V_O = 0; no load	T_A = 25°C		1.4	2.5	mA
V_{O1} / V_{O2}	Crosstalk attenuation	A_{VD} = 100	T_A = 25°C		120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
(2) T_A = –40°C to 85°C.
(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 1. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

6.14 Electrical Characteristics: TL071M, TL072M

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS [1] [2]		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		3	6	mV
			T_A = Full range			9	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	T_A = Full range		18		μV/°C
I_{IO}	Input offset current	V_O = 0	T_A = 25°C		5	100	pA
			T_A = Full range			20	nA
I_{IB}	Input bias current	V_O = 0	T_A = 25°C		65	200	pA
			T_A = Full range			50	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	T_A = 25°C	±12	±13.5		V
		R_L ≥ 10 kΩ	T_A = Full range	±12			
		R_L ≥ 2 kΩ		±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	T_A = 25°C	35	200		V/mV
			T_A = Full range	15			
B_1	Unity-gain bandwidth				3		MHz
r_i	Input resistance				10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(min)}$, V_O = 0, R_S = 50 Ω	T_A = 25°C	80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	T_A = 25°C	80	86		dB
I_{CC}	Supply current (each amplifier)	V_O = 0; no load	T_A = 25°C		1.4	2.5	mA
V_{O1} / V_{O2}	Crosstalk attenuation	A_{VD} = 100	T_A = 25°C		120		dB

(1) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 1. Pulse techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.
(2) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is T_A = –55°C to +125°C.

6.15 Electrical Characteristics: TL074M

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1) (2)		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		3	9	mV
			T_A = Full range			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	T_A = Full range		18		μV/°C
I_{IO}	Input offset current	V_O = 0	T_A = 25°C		5	100	pA
			T_A = Full range			20	nA
I_{IB}	Input bias current	V_O = 0	T_A = 25°C		65	200	pA
			T_A = Full range			20	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	T_A = 25°C	±12	±13.5		V
		R_L ≥ 10 kΩ	T_A = Full range	±12			
		R_L ≥ 2 kΩ		±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	T_A = 25°C	35	200		V/mV
			T_A = Full range	15			
B_1	Unity-gain bandwidth				3		MHz
r_i	Input resistance				10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(min)}$, V_O = 0, R_S = 50 Ω	T_A = 25°C	80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	T_A = 25°C	80	86		dB
I_{CC}	Supply current (each amplifier)	V_O = 0; no load	T_A = 25°C		1.4	2.5	mA
V_{O1} / V_{O2}	Crosstalk attenuation	A_{VD} = 100	T_A = 25°C		120		dB

(1) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 1. Pulse techniques that maintain the junction temperature as close to the ambient temperature as possible must be used .
(2) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is T_A = –55°C to +125°C.

6.16 Switching Characteristics: TL07xM

$V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V C_L = 100 pF	R_L = 2 kΩ See Figure 21	5	13		V/μs
t_r	Rise-time overshoot factor	V_I = 20 V C_L = 100 pF	R_L = 2 kΩ See Figure 21		0.1		μs
					20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18		nV/√Hz
			f = 10 Hz to 10 kHz		4		μV
I_n	Equivalent input noise current	R_S = 20 Ω	f = 1 kHz		0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V R_L ≥ 2 kΩ f = 1 kHz	A_{VD} = 1 RS ≤ 1 kΩ		0.003%		

6.17 Switching Characteristics: TL07xC, TL07xAC, TL07xBC, TL07xI

$V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V C_L = 100 pF	R_L = 2 kΩ See Figure 21	8	13		V/μs
t_r	Rise-time overshoot factor	V_I = 20 V C_L = 100 pF	R_L = 2 kΩ See Figure 21		0.1		μs
					20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18		nV/√Hz
			f = 10 Hz to 10 kHz		4		μV
I_n	Equivalent input noise current	R_S = 20 Ω	f = 1 kHz		0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V R_L ≥ 2 kΩ f = 1 kHz	A_{VD} = 1 RS ≤ 1 kΩ		0.003%		

6.18 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Table 1. Typical Characteristics: Table of Graphs

			FIGURE
I_{IB}	Input bias current	versus free-air temperature	Figure 1
V_{OM}	Maximum peak output voltage	versus frequency	Figure 2
			Figure 3
			Figure 4
		versus free-air temperature	Figure 5
		versus load resistance	Figure 6
		versus supply voltage	Figure 7
A_{VD}	Large signal differential voltage amplification	versus free-air temperature	Figure 8
		versus load resistance	Figure 9
	Phase shift	versus frequency	Figure 9
	Normalized unity-gain bandwidth	versus free-air temperature	Figure 10
	Normalized phase shift	versus free-air temperature	Figure 10
CMRR	Common-mode rejection ratio	versus free-air temperature	Figure 11
	Input offset voltage change	versus common-mode voltage	Figure 20
I_{CC}	Supply current	versus free-air temperature	Figure 13
		versus supply voltage	Figure 12
P_D	Total power dissipation	versus free-air temperature	Figure 14
	Normalized slew rate	versus free-air temperature	Figure 15
V_n	Equivalent input noise voltage	versus frequency	Figure 16
THD	Total harmonic distortion	versus frequency	Figure 17
	Large-signal pulse response	versus time	Figure 18
V_O	Output voltage	versus elapsed time	Figure 19

6.18.1 Typical Characteristics

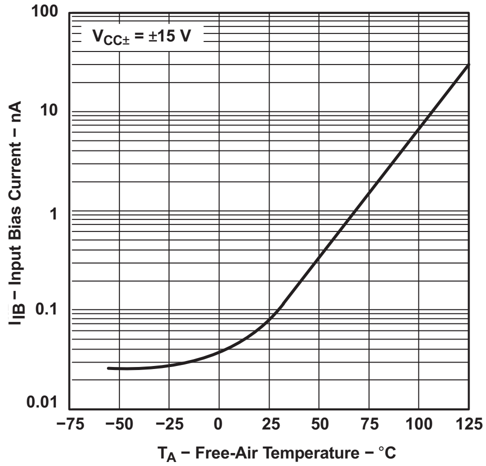


Figure 1. Input Bias Current vs Free-Air Temperature

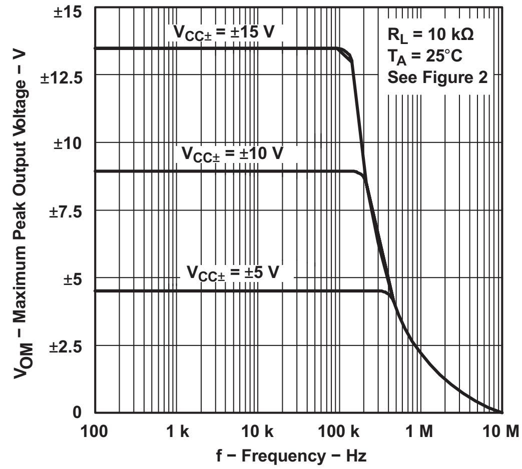


Figure 2. Maximum Peak Output Voltage vs Frequency

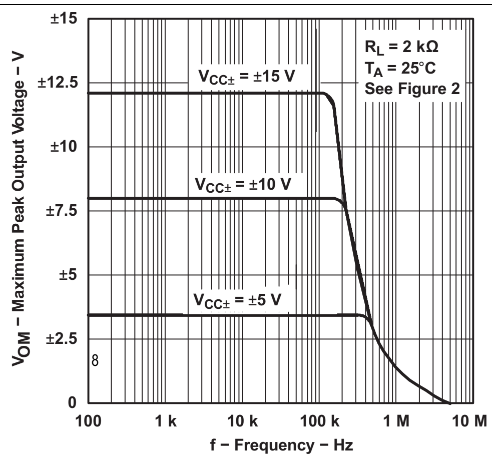


Figure 3. Maximum Peak Output Voltage vs Frequency

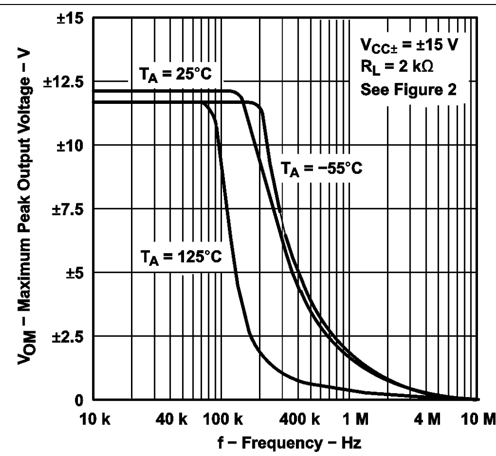


Figure 4. Maximum Peak Output Voltage vs Frequency

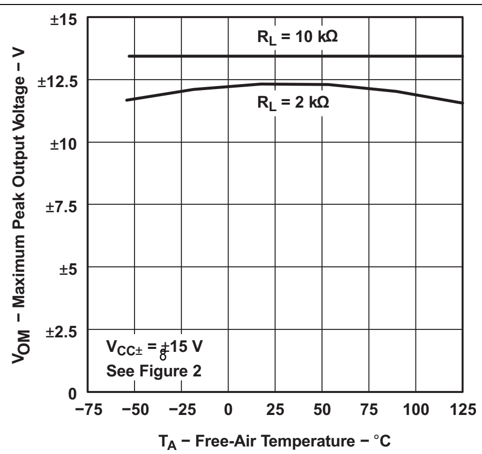


Figure 5. Maximum Peak Output Voltage vs Free-Air Temperature

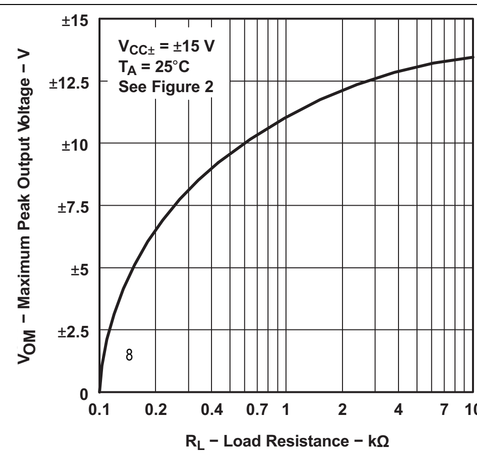


Figure 6. Maximum Peak Output Voltage vs Load Resistance

Typical Characteristics (continued)

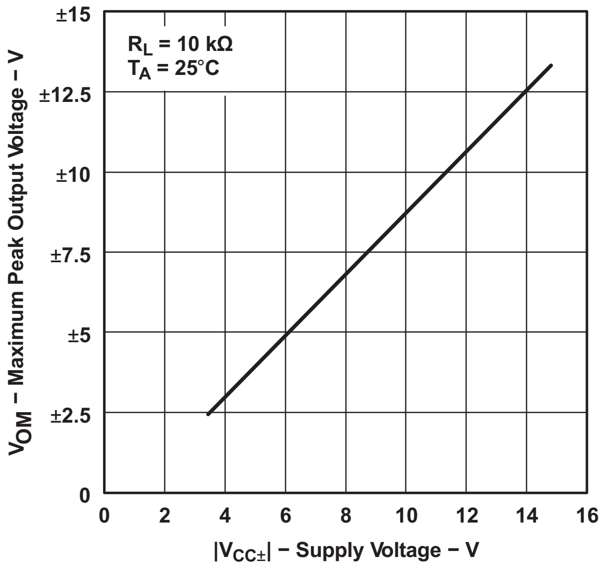


Figure 7. Maximum Peak Output Voltage vs Supply Voltage

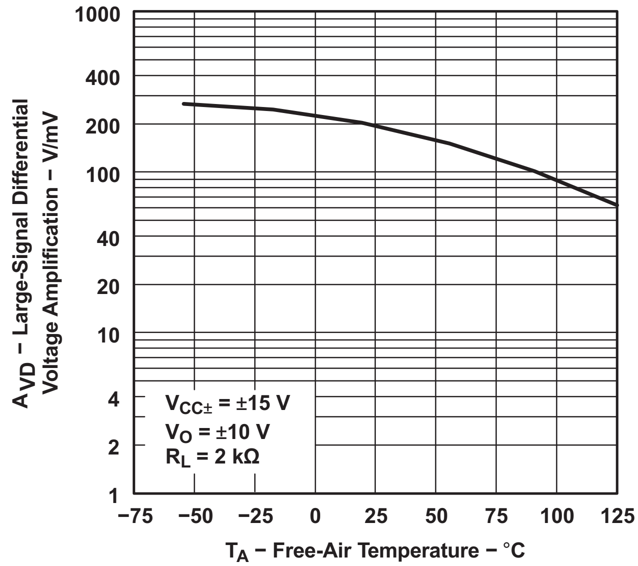


Figure 8. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

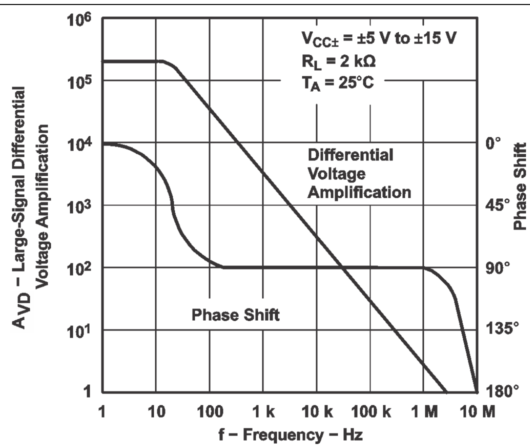


Figure 9. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

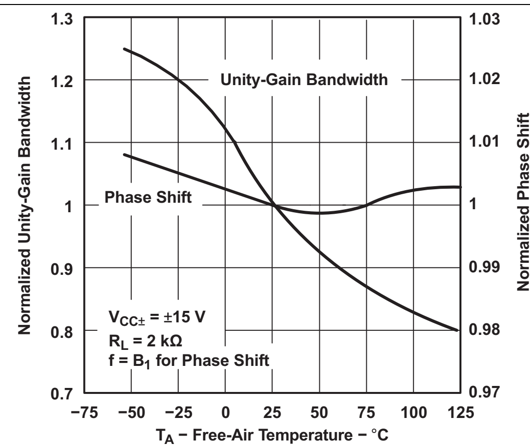


Figure 10. Normalized Unity-Gain Bandwidth and Phase Shift vs Free-Air Temperature

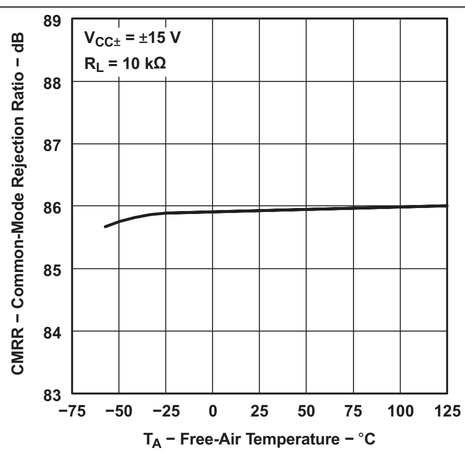


Figure 11. Common-Mode Rejection Ratio vs Free-Air Temperature

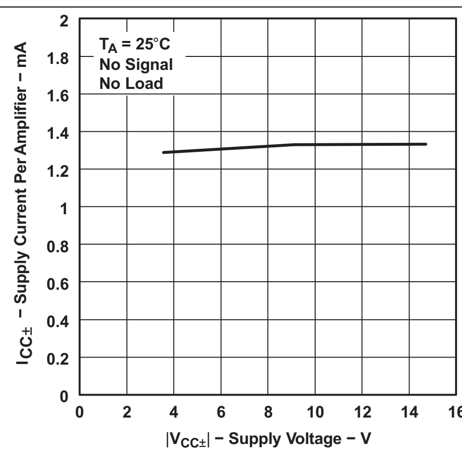


Figure 12. Supply Current Per Amplifier vs Supply Voltage

Typical Characteristics (continued)

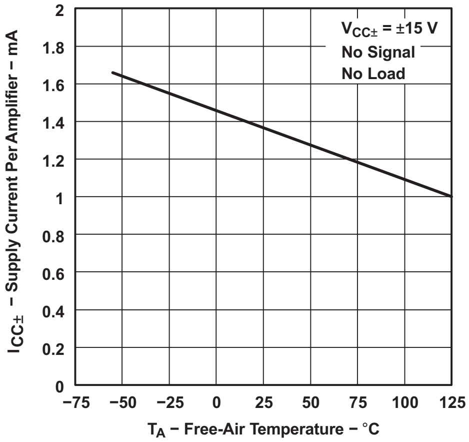


Figure 13. Supply Current Per Amplifier vs Free-Air Temperature

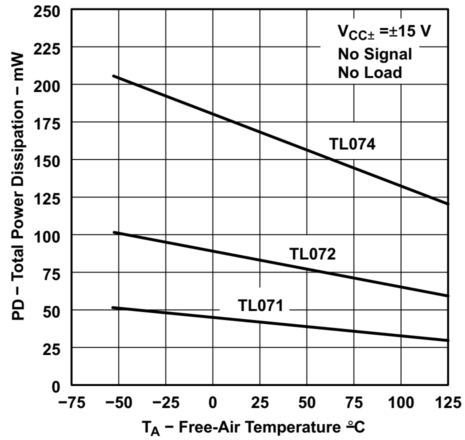


Figure 14. Total Power Dissipation vs Free-Air Temperature

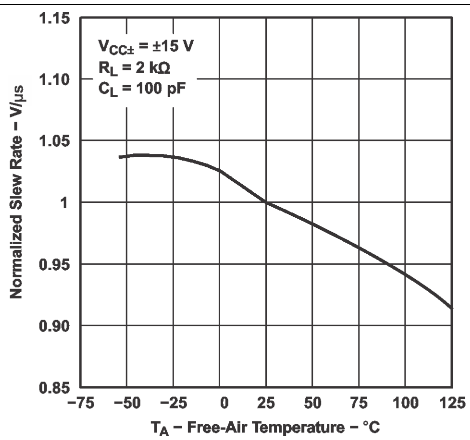


Figure 15. Normalized Slew Rate vs Free-Air Temperature

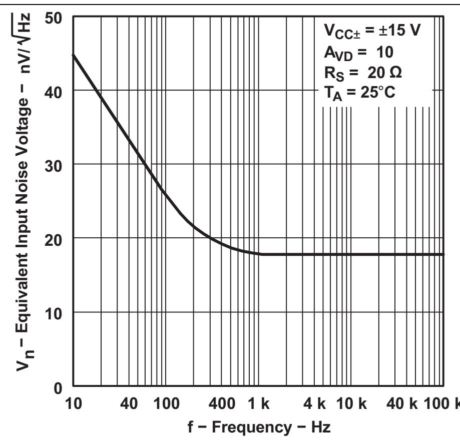


Figure 16. Equivalent Input Noise Voltage vs Frequency

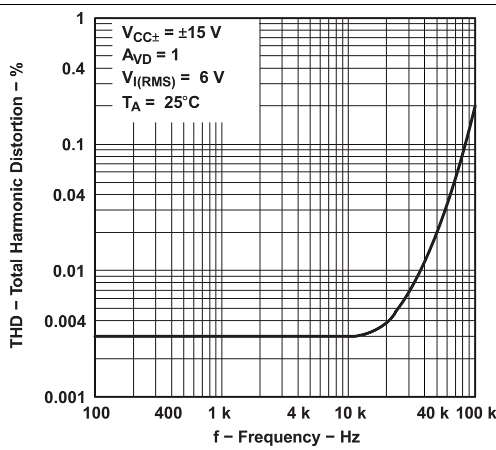


Figure 17. Total Harmonic Distortion vs Frequency

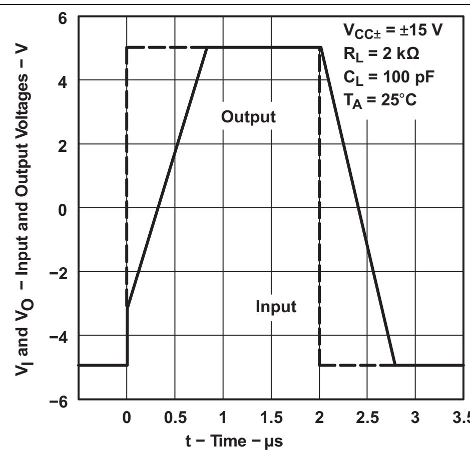


Figure 18. Voltage-Follower Large-Signal Pulse Response

Typical Characteristics (continued)

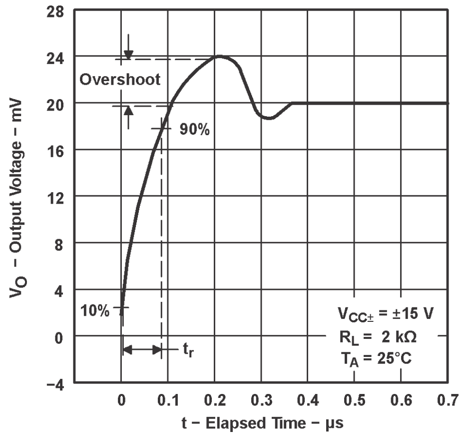


Figure 19. Output Voltage vs Elapsed Time

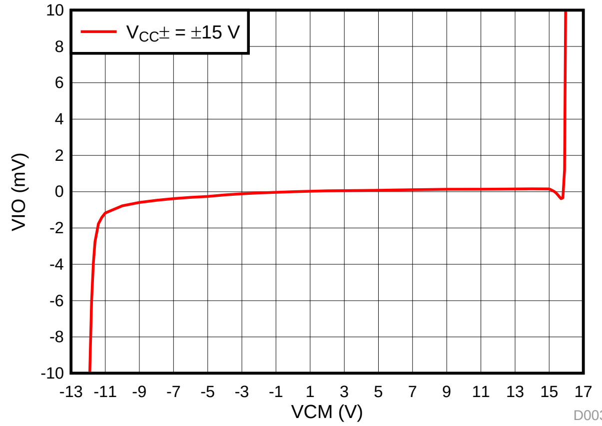


Figure 20. V_{IO} vs V_{CM}

6.1 Parameter Measurement Information

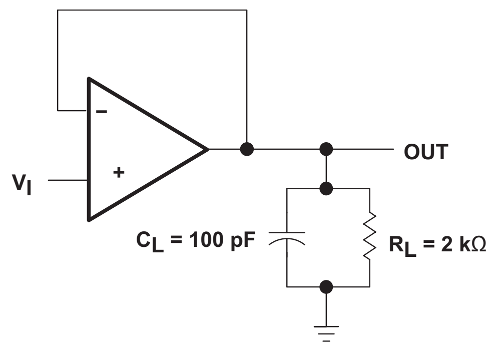


Figure 21. Unity-Gain Amplifier

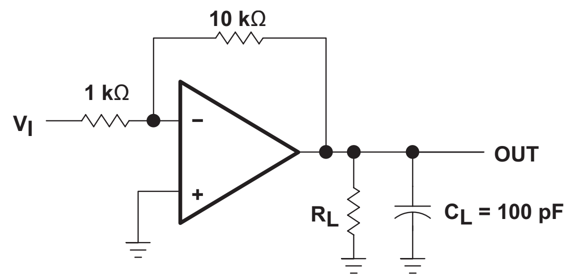


Figure 22. Gain-of-10 Inverting Amplifier

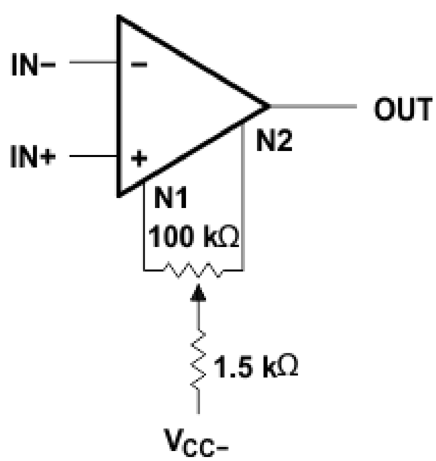


Figure 23. Input Offset-Voltage Null Circuit

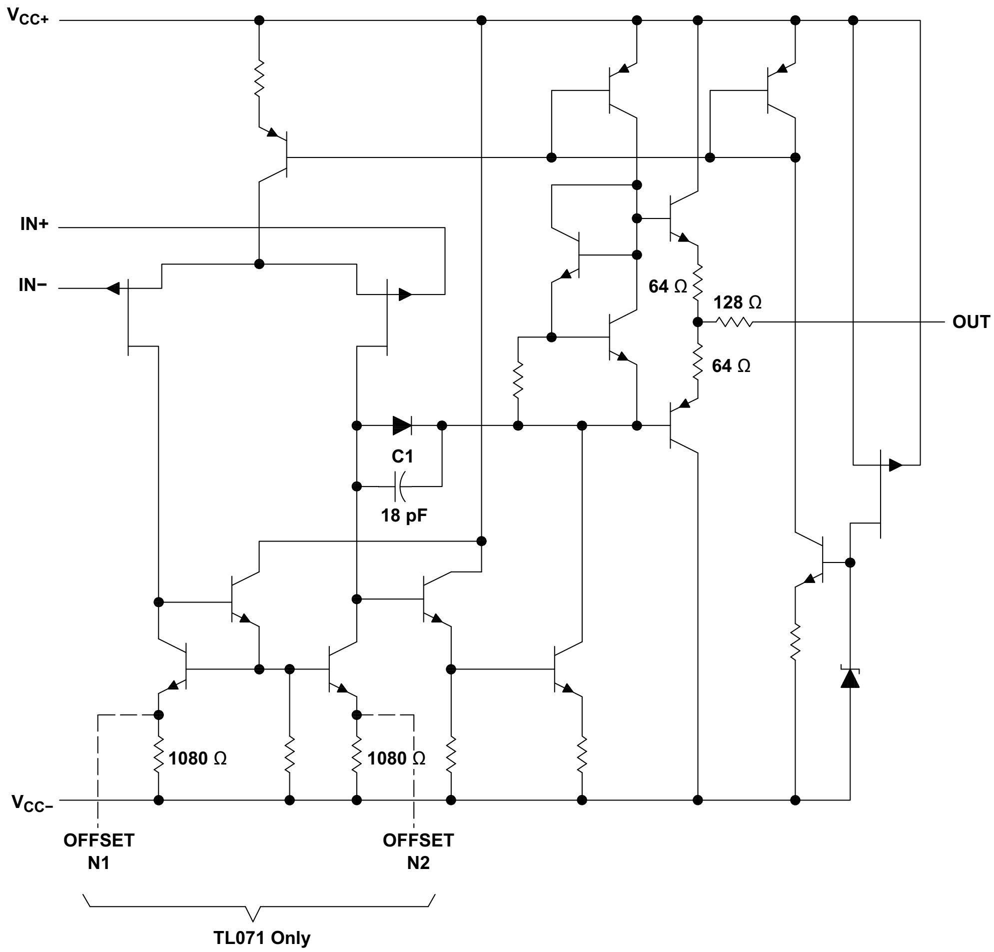
7 Detailed Description

7.1 Overview

The JFET-input operational amplifiers in the TL07xx series are similar to the TL08x series, with low input bias and offset currents, and a fast slew rate. The low harmonic distortion and low noise make the TL07xx series ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to +85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to +125°C.

7.2 Functional Block Diagram



All component values shown are nominal.

COMPONENT COUNT†			
COMPONENT TYPE	TL071	TL072	TL074
Resistors	11	22	44
Transistors	14	28	56
JFET	2	4	6
Diodes	1	2	4
Capacitors	1	2	4
epi-FET	1	2	4

† Includes bias and trim circuitry

7.3 Feature Description

7.3.1 Total Harmonic Distortion

Harmonic distortions to an audio signal are created by electronic components in a circuit. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. These devices have a very low THD of 0.003% meaning that the TL07x device adds little harmonic distortion when used in audio signal applications.

7.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change the output when there is a change on the input. These devices have a 13-V/μs slew rate.

7.4 Device Functional Modes

These devices are powered on when the supply is connected. These devices can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes the voltage a negative voltage. In the same manner, the amplifier makes negative voltages positive.

8.2 Typical Application

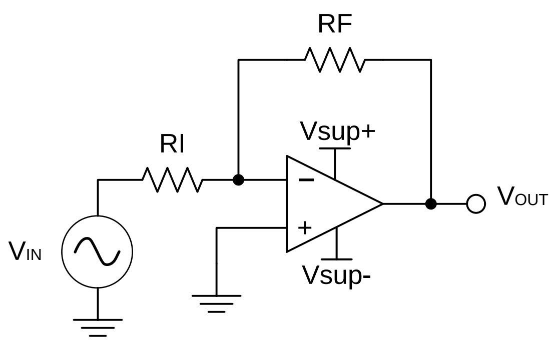


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Figure 24. Inverting Amplifier

8.2.1 Design Requirements

The supply voltage must be selected so the supply voltage is larger than the input voltage range and output range. For instance, this application scales a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

8.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_V = \frac{VOUT}{VIN} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, select a value for RI or RF. Selecting a value in the kilohm range is desirable because the amplifier circuit uses currents in the milliamp range. This ensures the part does not draw too much current. This example uses 10 kΩ for RI which means 36 kΩ is used for RF. This is determined by Equation 3.

$$A_V = -\frac{RF}{RI} \quad (3)$$

Typical Application (continued)

8.2.3 Application Curve

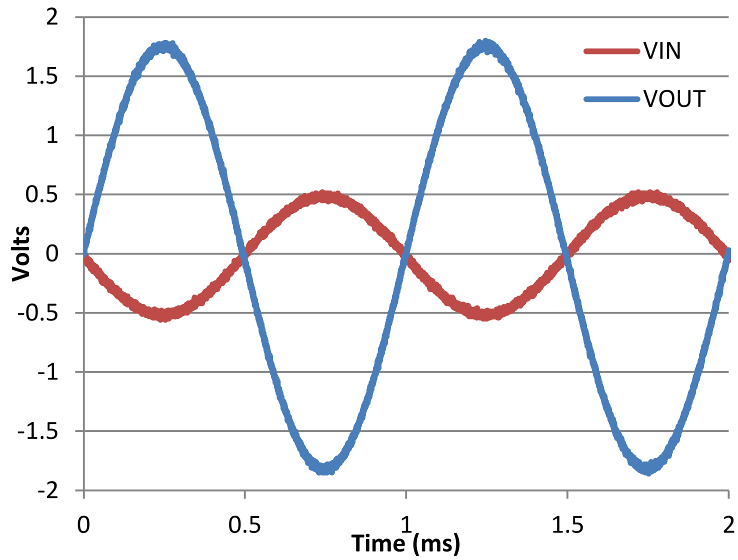

Figure 25. Input and Output Voltages of the Inverting Amplifier

8.3 Unity Gain Buffer

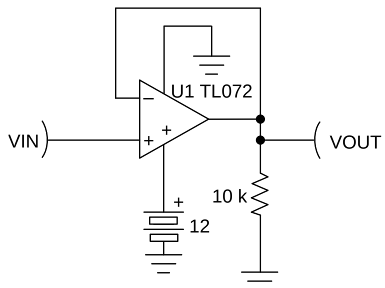

Figure 26. Single-Supply Unity Gain Amplifier

8.3.1 Design Requirements

- V_{CC} must be within valid range per *Recommended Operating Conditions*. This example uses a value of 12 V for V_{CC}.
- Input voltage must be within the recommended common-mode range, as shown in *Recommended Operating Conditions*. The valid common-mode range is 4 V to 12 V (V_{CC-} + 4 V to V_{CC+}.
- Output is limited by output range, which is typically 1.5 V to 10.5 V, or V_{CC-} + 1.5 V to V_{CC+} – 1.5 V.

8.3.2 Detailed Design Procedure

- Avoid input voltage values below 1 V to prevent phase reversal where output goes high.
- Avoid input values below 4 V to prevent degraded V_{IO} that results in an apparent gain greater than 1. This may cause instability in some second-order filter designs.

Unity Gain Buffer (continued)

8.3.3 Application Curves

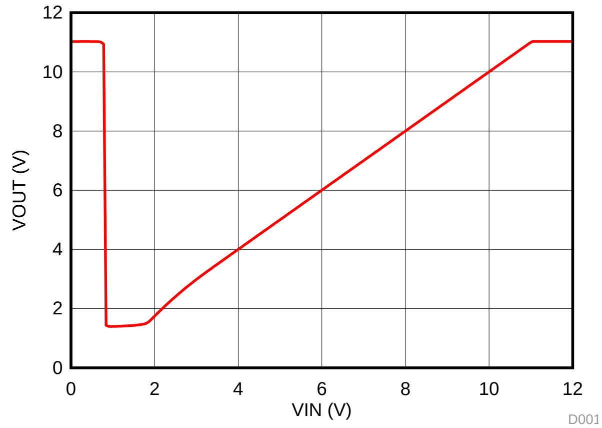

Figure 27. Output Voltage vs Input Voltage

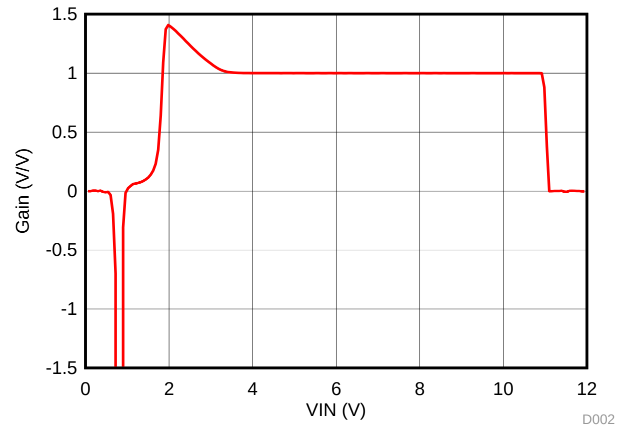

Figure 28. Gain vs Input Voltage

8.4 System Examples

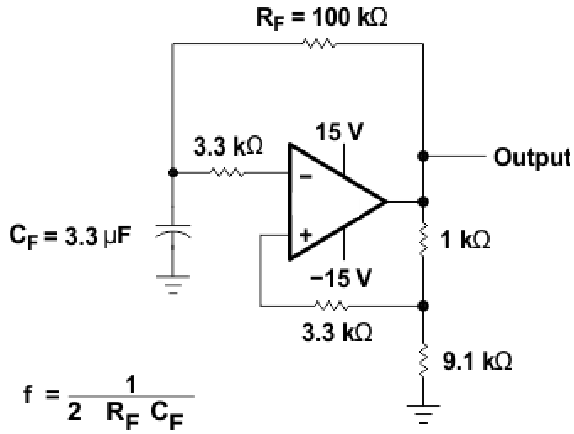

Figure 29. 0.5-Hz Square-Wave Oscillator

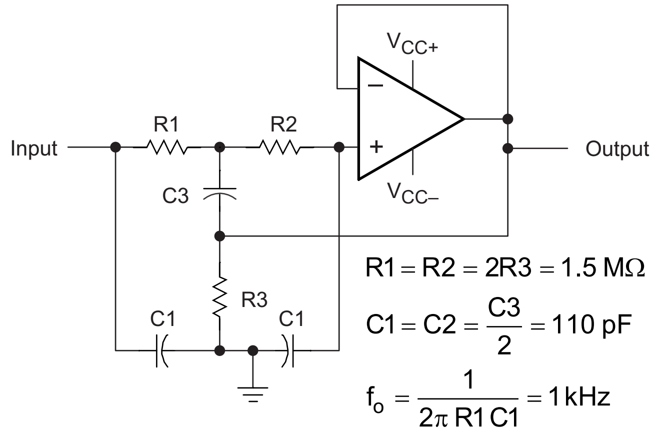

Figure 30. High-Q Notch Filter

System Examples (continued)

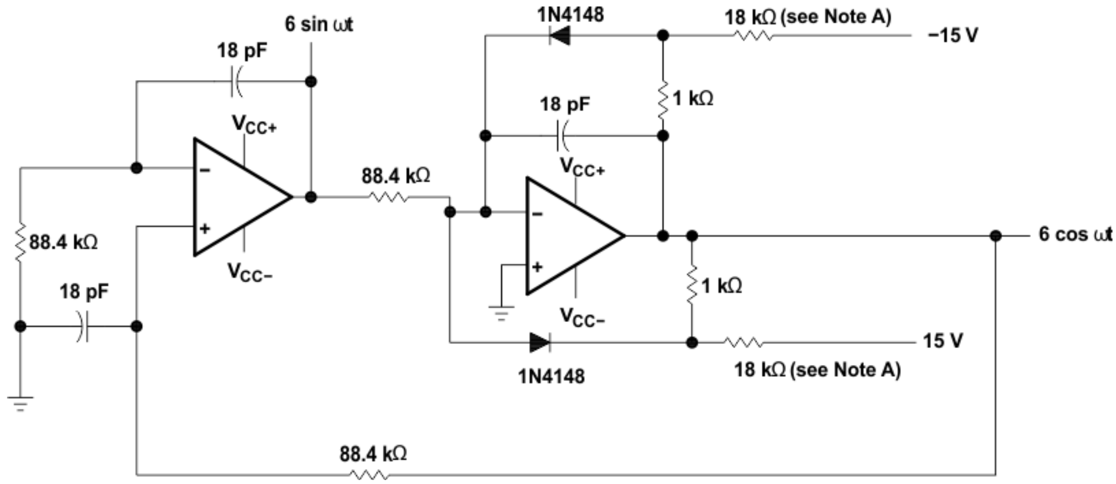

Figure 31. 100-kHz Quadrature Oscillator

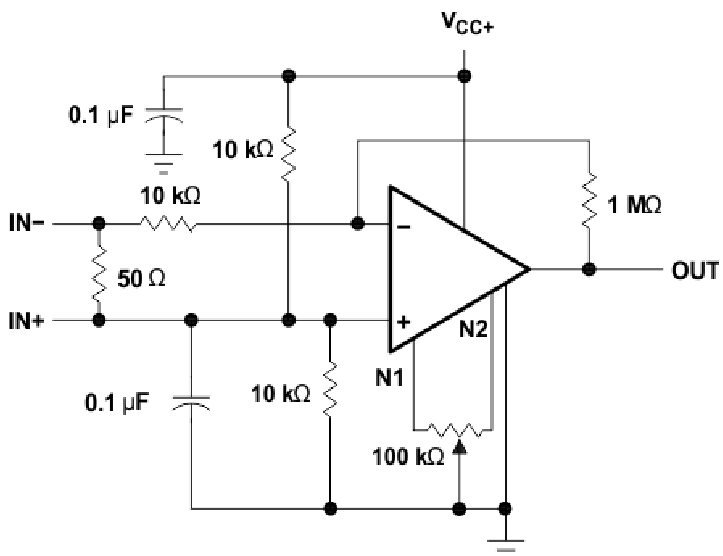

Figure 32. AC Amplifier

9 Power Supply Recommendations

CAUTION

Supply voltages larger than 36 V for a single-supply or outside the range of ±18 V for a dual-supply can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  – Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

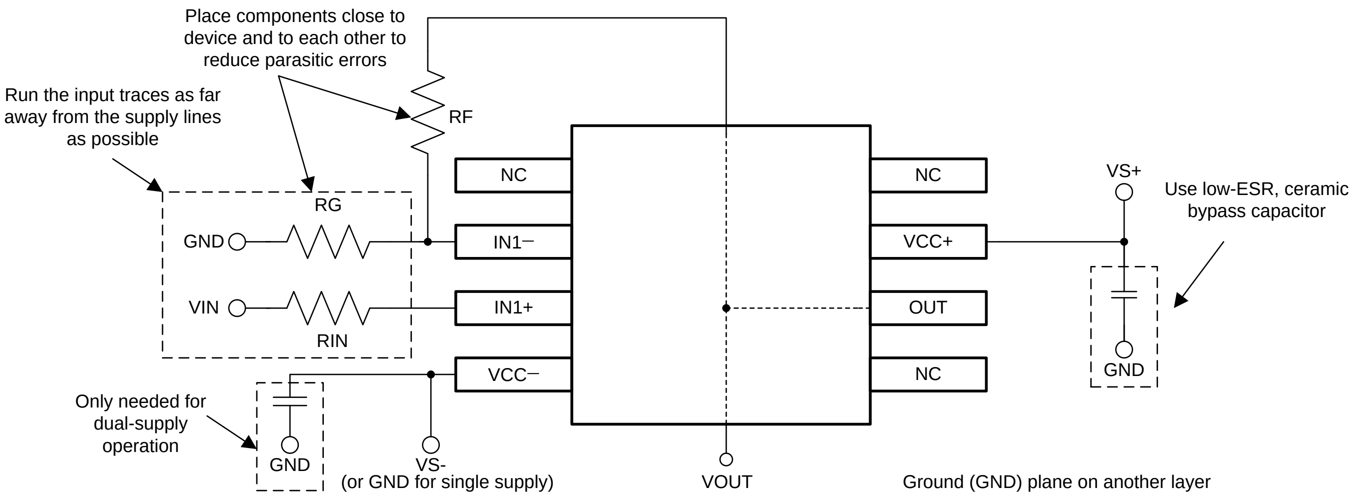

Figure 33. Operational Amplifier Board Layout for Noninverting Configuration

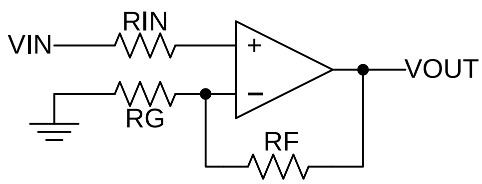

Figure 34. Operational Amplifier Schematic for Noninverting Configuration

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

Circuit Board Layout Techniques (SLOA089)

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL071	Click here	Click here	Click here	Click here	Click here
TL071A	Click here	Click here	Click here	Click here	Click here
TL071B	Click here	Click here	Click here	Click here	Click here
TL072	Click here	Click here	Click here	Click here	Click here
TL072A	Click here	Click here	Click here	Click here	Click here
TL072B	Click here	Click here	Click here	Click here	Click here
TL072M	Click here	Click here	Click here	Click here	Click here
TL074	Click here	Click here	Click here	Click here	Click here
TL074A	Click here	Click here	Click here	Click here	Click here
TL074B	Click here	Click here	Click here	Click here	Click here
TL074M	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
81023052A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023052A TL072MFKB	Samples
8102305HA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102305HA TL072M	Samples
8102305PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102305PA TL072M	Samples
81023062A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023062A TL074MFKB	Samples
8102306CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102306CA TL074MJB	Samples
8102306DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102306DA TL074MWB	Samples
JM38510/11905BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /11905BPA	Samples
M38510/11905BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /11905BPA	Samples
TL071ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	Samples
TL071ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	Samples
TL071ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	Samples
TL071ACP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL071ACP	Samples
TL071BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC	Samples
TL071BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC	Samples
TL071BCP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL071BCP	Samples
TL071CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples
TL071CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL071CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples
TL071CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples
TL071CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL071CP	Samples
TL071CPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL071CP	Samples
TL071CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T071	Samples
TL071ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	Samples
TL071IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	Samples
TL071IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	Samples
TL071IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL071IP	Samples
TL072ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL072ACP	Samples
TL072ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL072ACP	Samples
TL072BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL072BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL072BCP	Samples
TL072BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL072BCP	Samples
TL072CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL072CP	Samples
TL072CPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL072CP	Samples
TL072CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL072CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL072IP	Samples
TL072IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL072IP	Samples
TL072MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023052A TL072MFKB	Samples
TL072MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TL072MJG	Samples
TL072MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102305PA TL072M	Samples
TL072MUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102305HA TL072M	Samples
TL074ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL074ACN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL074ACN	Samples
TL074ACNE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL074ACN	Samples
TL074ACNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074A	Samples
TL074BCD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL074BCN	Samples
TL074BCNE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL074BCN	Samples
TL074CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CDBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL074CN	Samples
TL074CNE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL074CN	Samples
TL074CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL074CNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074	Samples
TL074CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL074IN	Samples
TL074MFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	TL074MFK	Samples
TL074MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81023062A TL074MFKB	Samples
TL074MJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	TL074MJ	Samples
TL074MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102306CA TL074MJB	Samples
TL074MWB	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8102306DA TL074MWB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TL072, TL072M, TL074, TL074M :

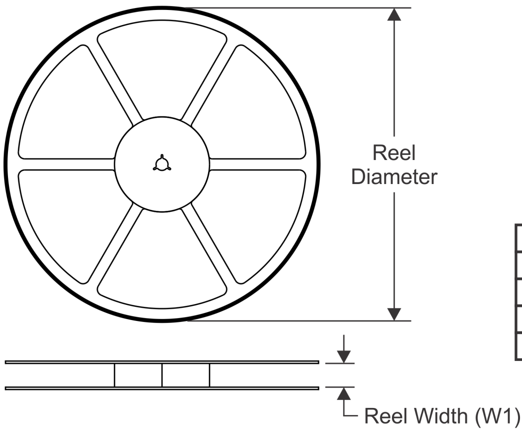
- Catalog: TL072, TL074
- Enhanced Product: TL072-EP, TL072-EP, TL074-EP, TL074-EP
- Military: TL072M, TL074M

NOTE: Qualified Version Definitions:

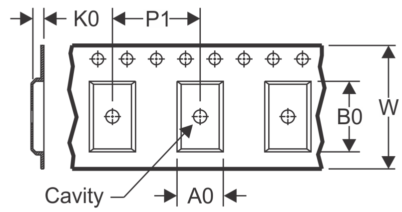
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

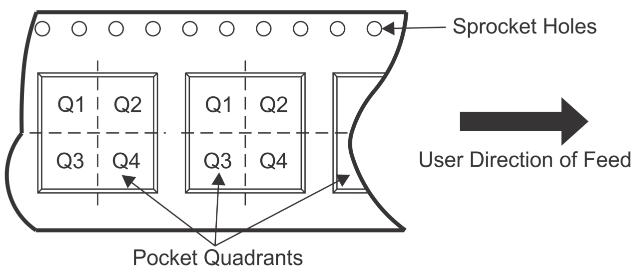


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

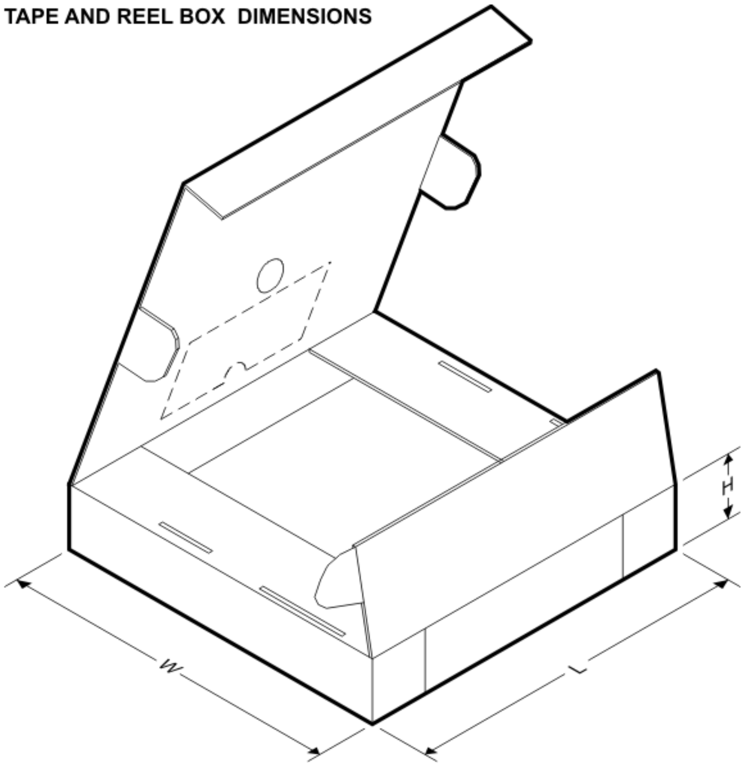


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL071ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL074ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074ACNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL074BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL074IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



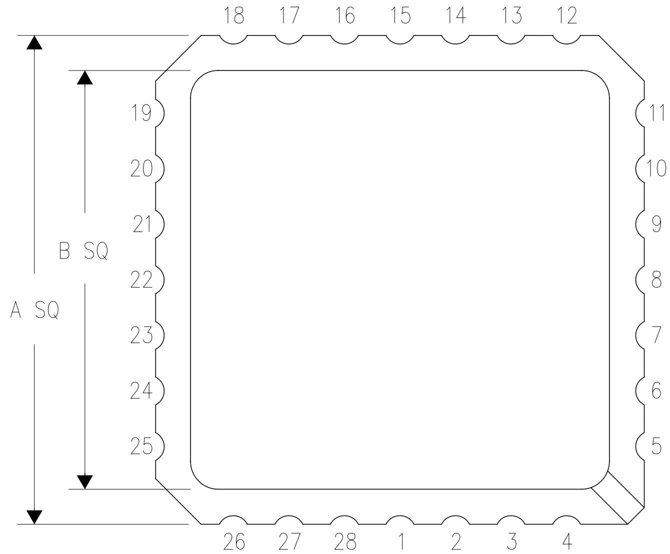
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL071ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL071CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL072CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL072IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072IDR	SOIC	D	8	2500	367.0	367.0	35.0
TL074ACDR	SOIC	D	14	2500	333.2	345.9	28.6
TL074ACNSR	SO	NS	14	2000	367.0	367.0	38.0
TL074BCDR	SOIC	D	14	2500	333.2	345.9	28.6
TL074CDR	SOIC	D	14	2500	333.2	345.9	28.6

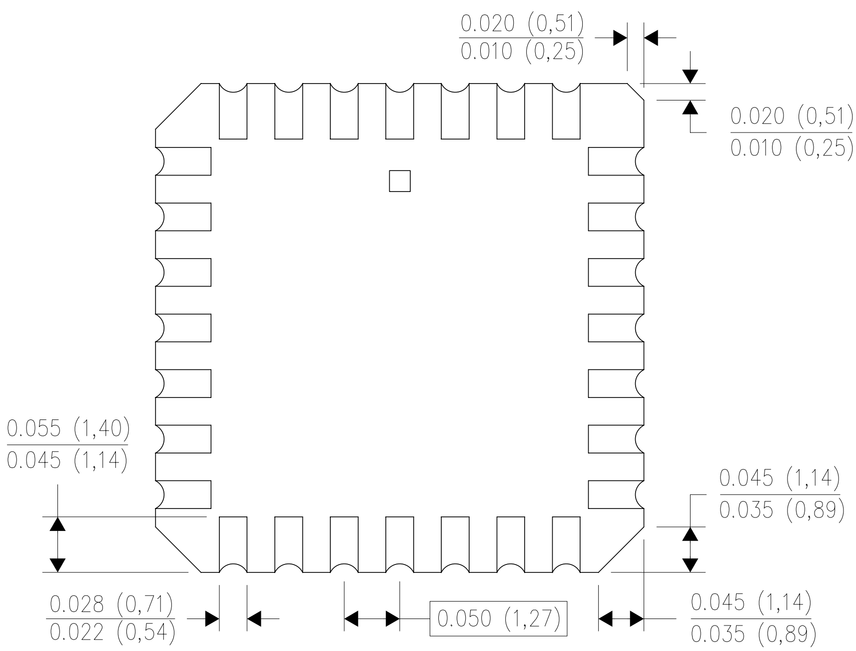
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL074CDRG4	SOIC	D	14	2500	333.2	345.9	28.6
TL074CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TL074IDR	SOIC	D	14	2500	333.2	345.9	28.6

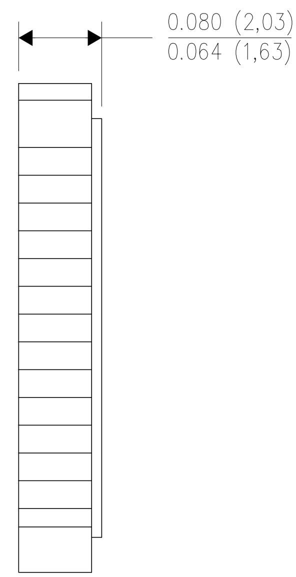
FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



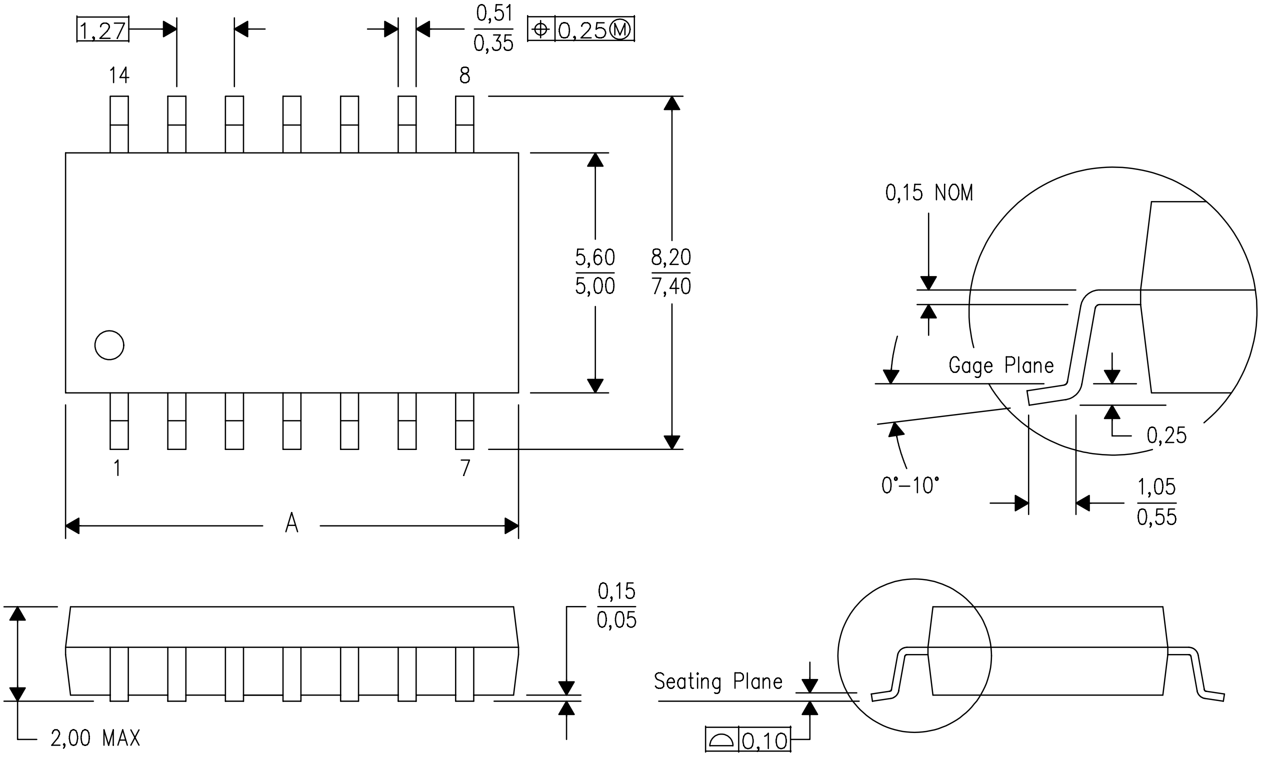


4040140/D 01/11

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

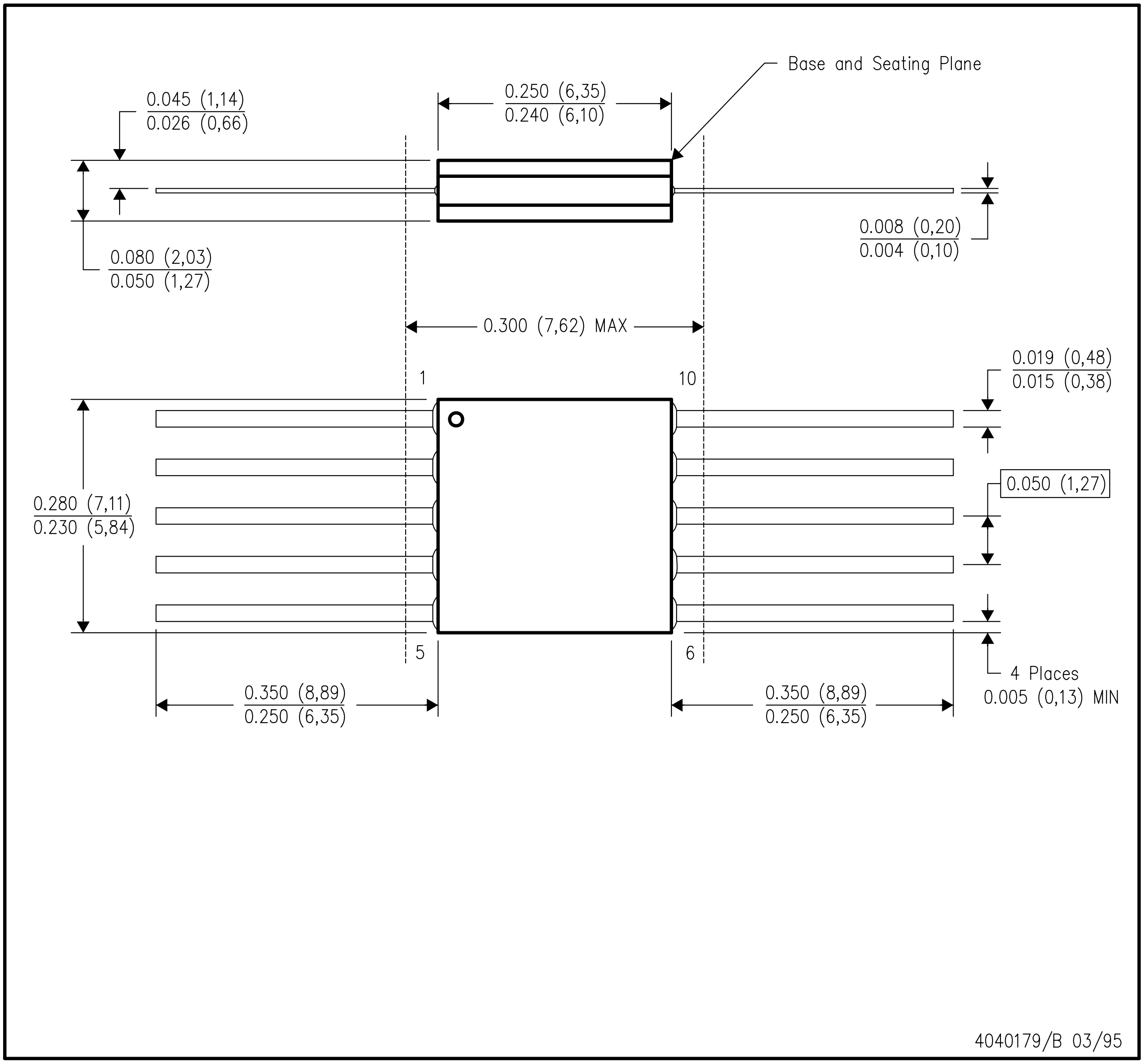


PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

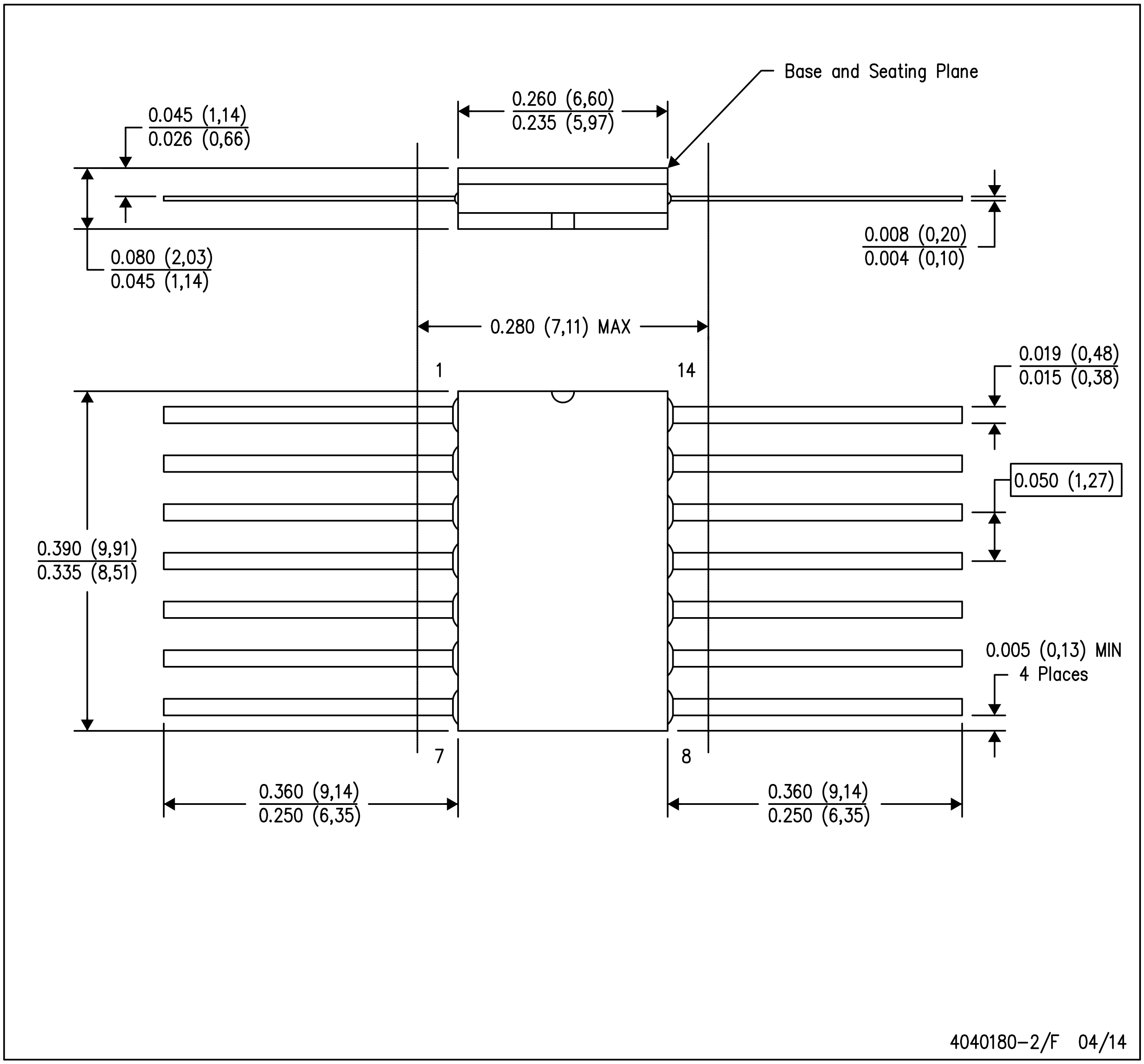
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

U (S-GDFP-F10) CERAMIC DUAL FLATPACK



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

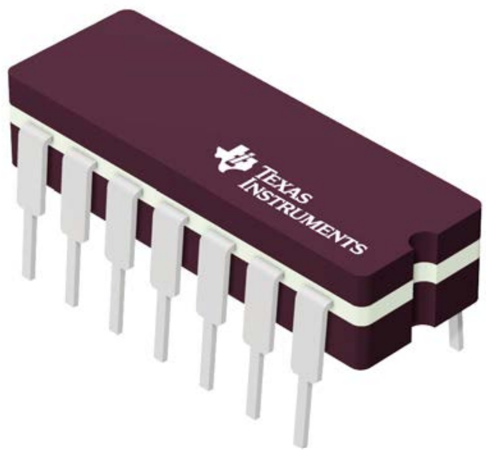
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



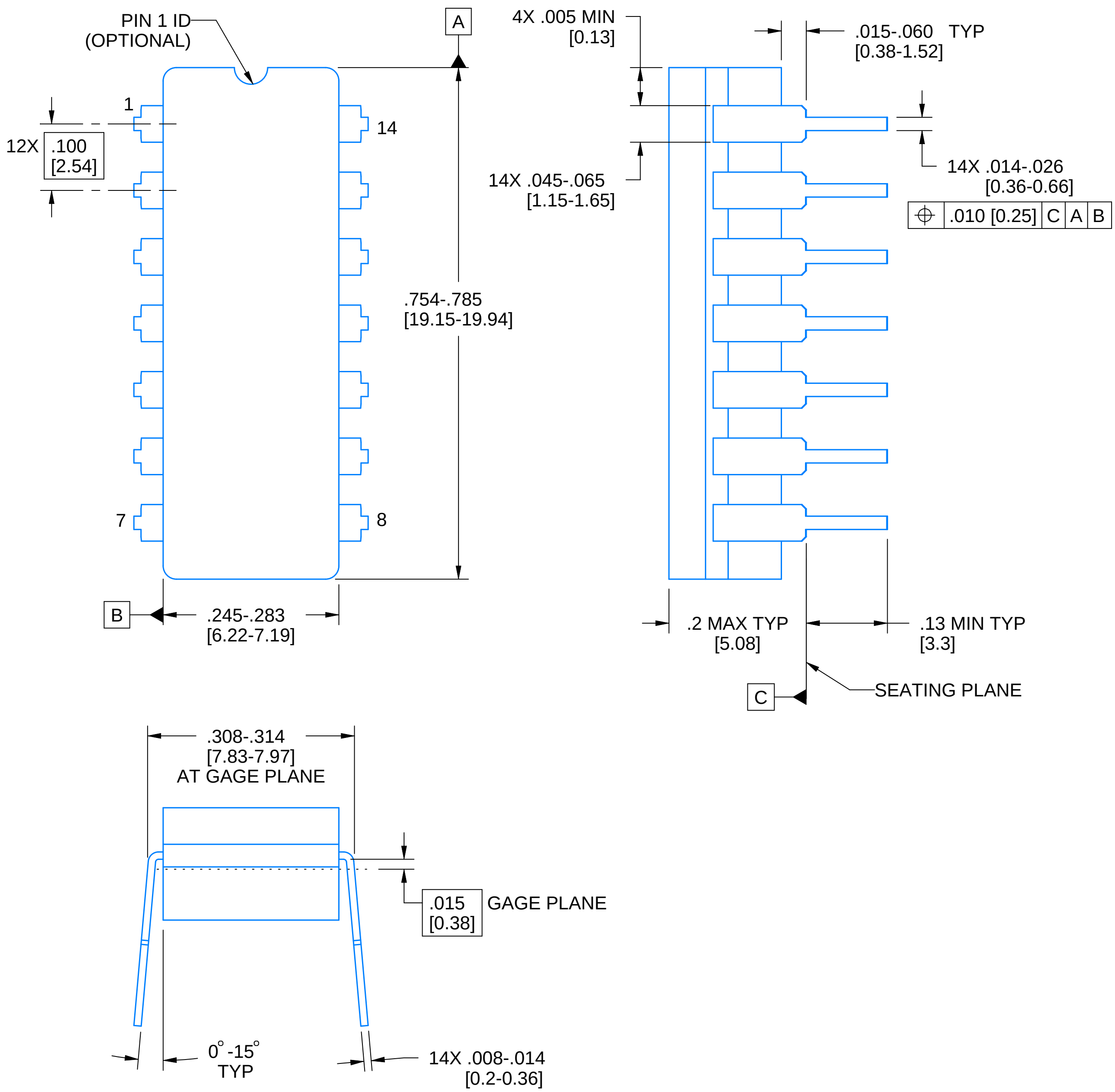
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



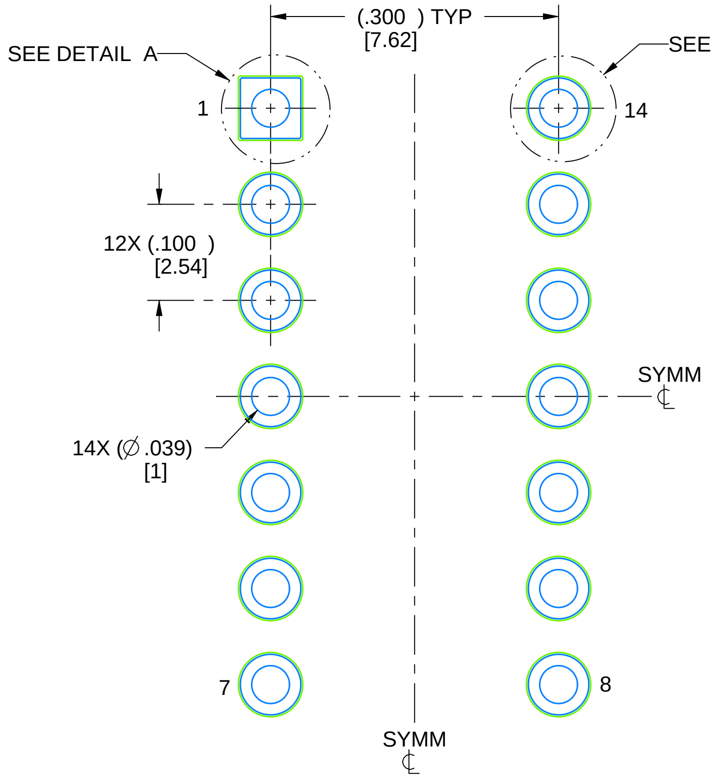
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



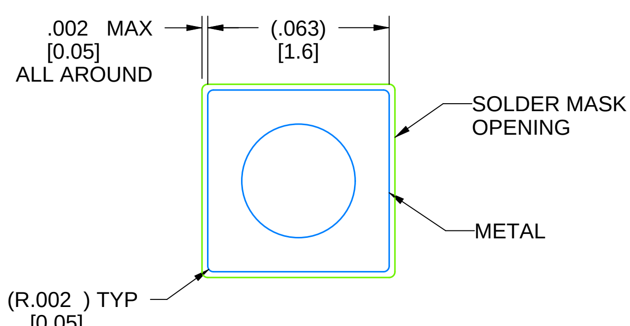
4214771/A 05/2017

NOTES:

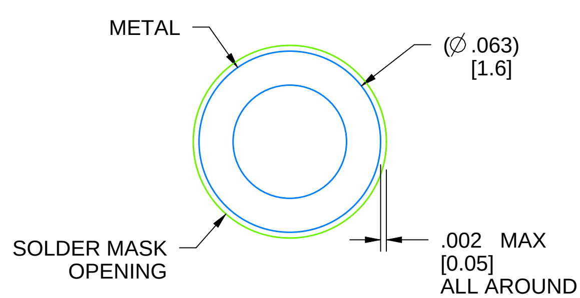
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



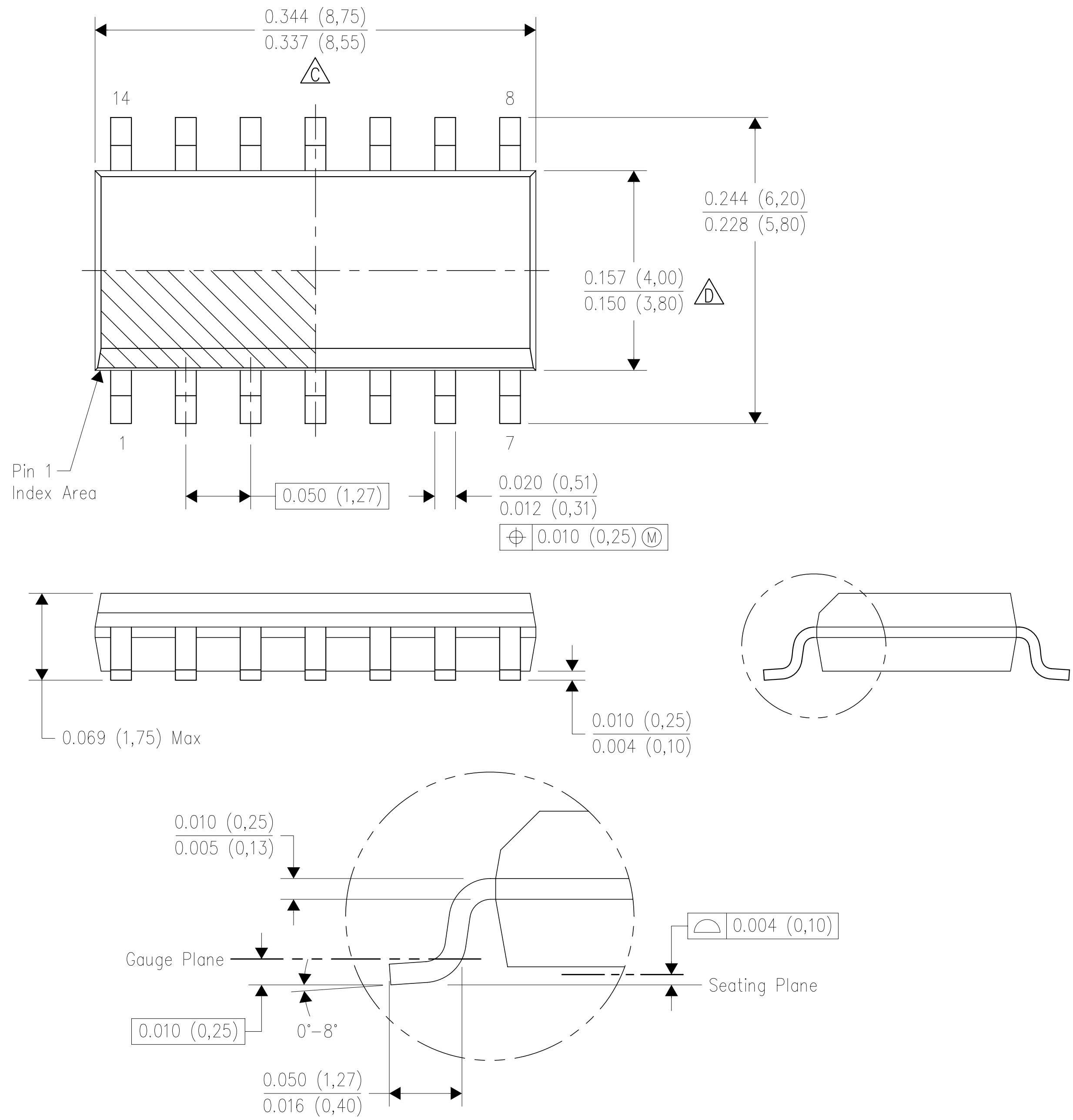
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

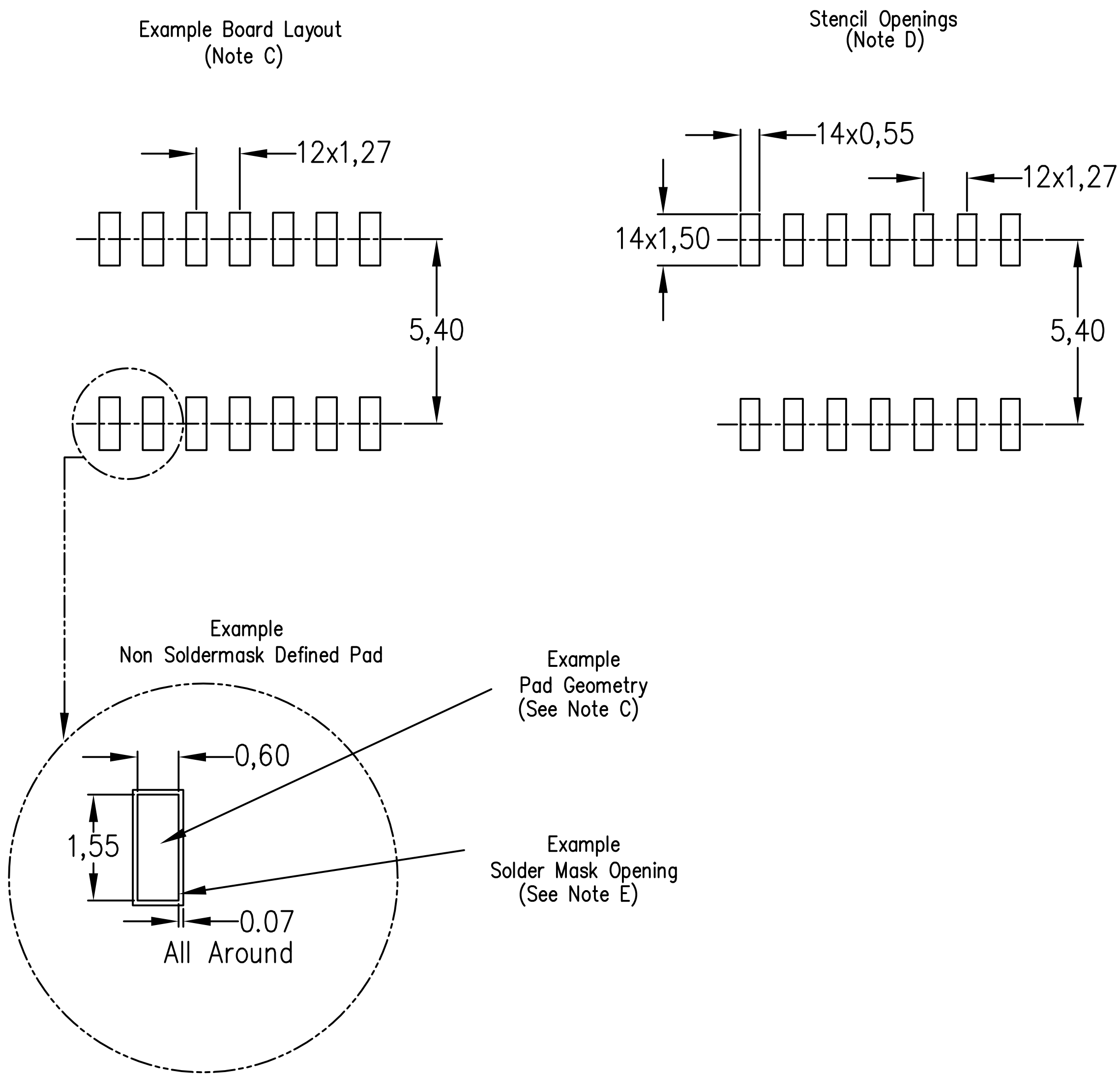
D (R-PDSO-G14) PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

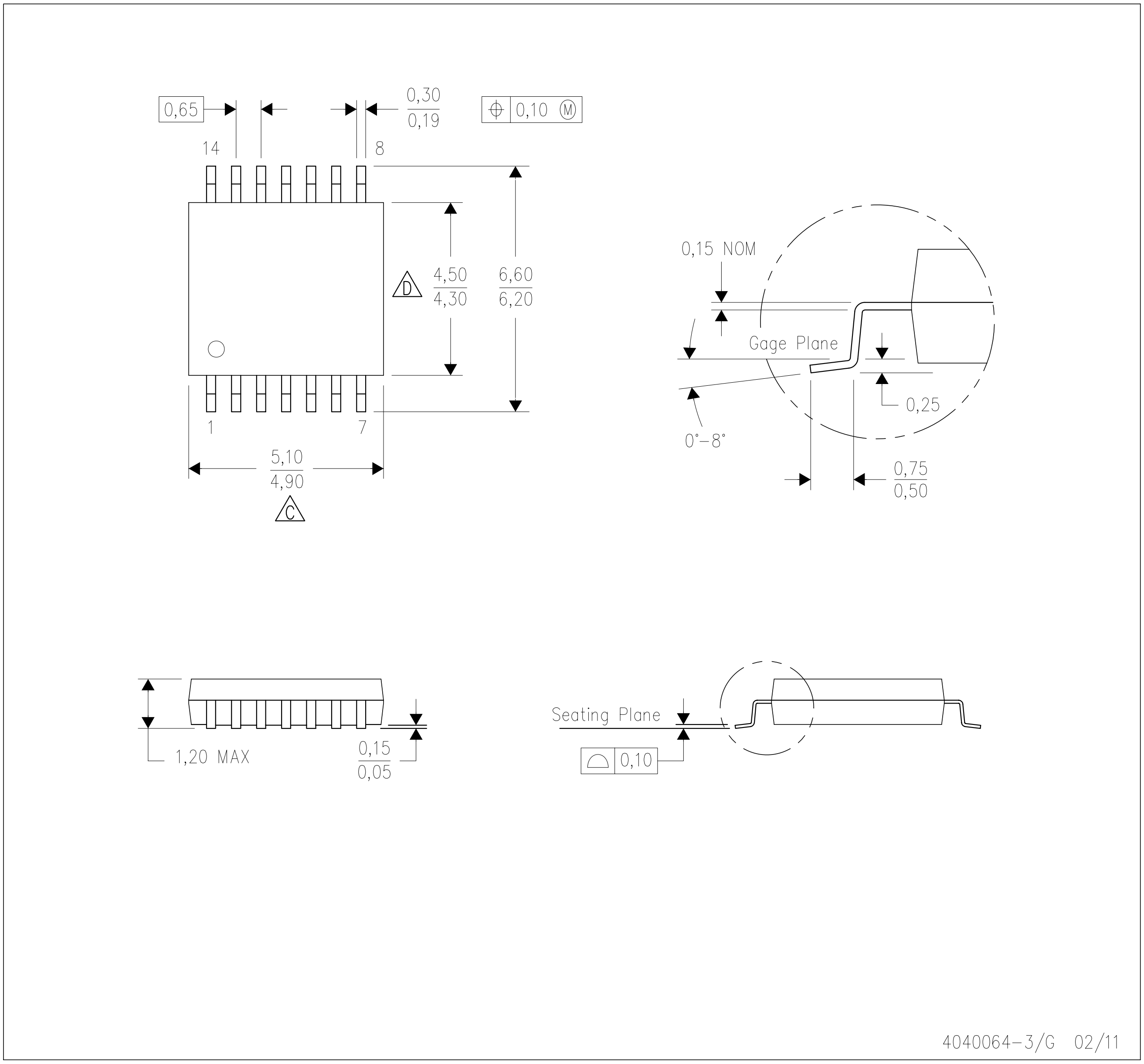
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4211283–3/E 08/12

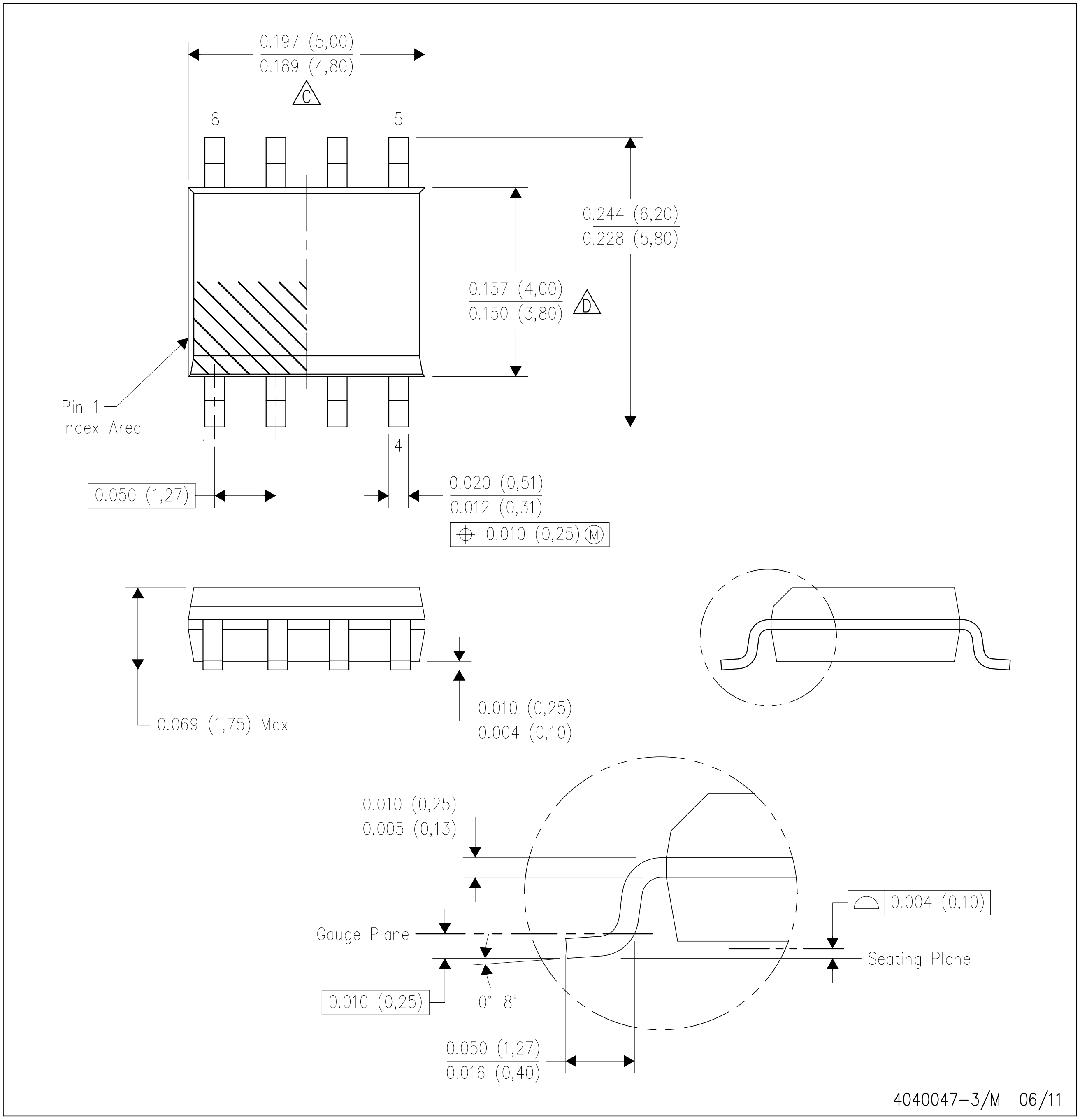
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



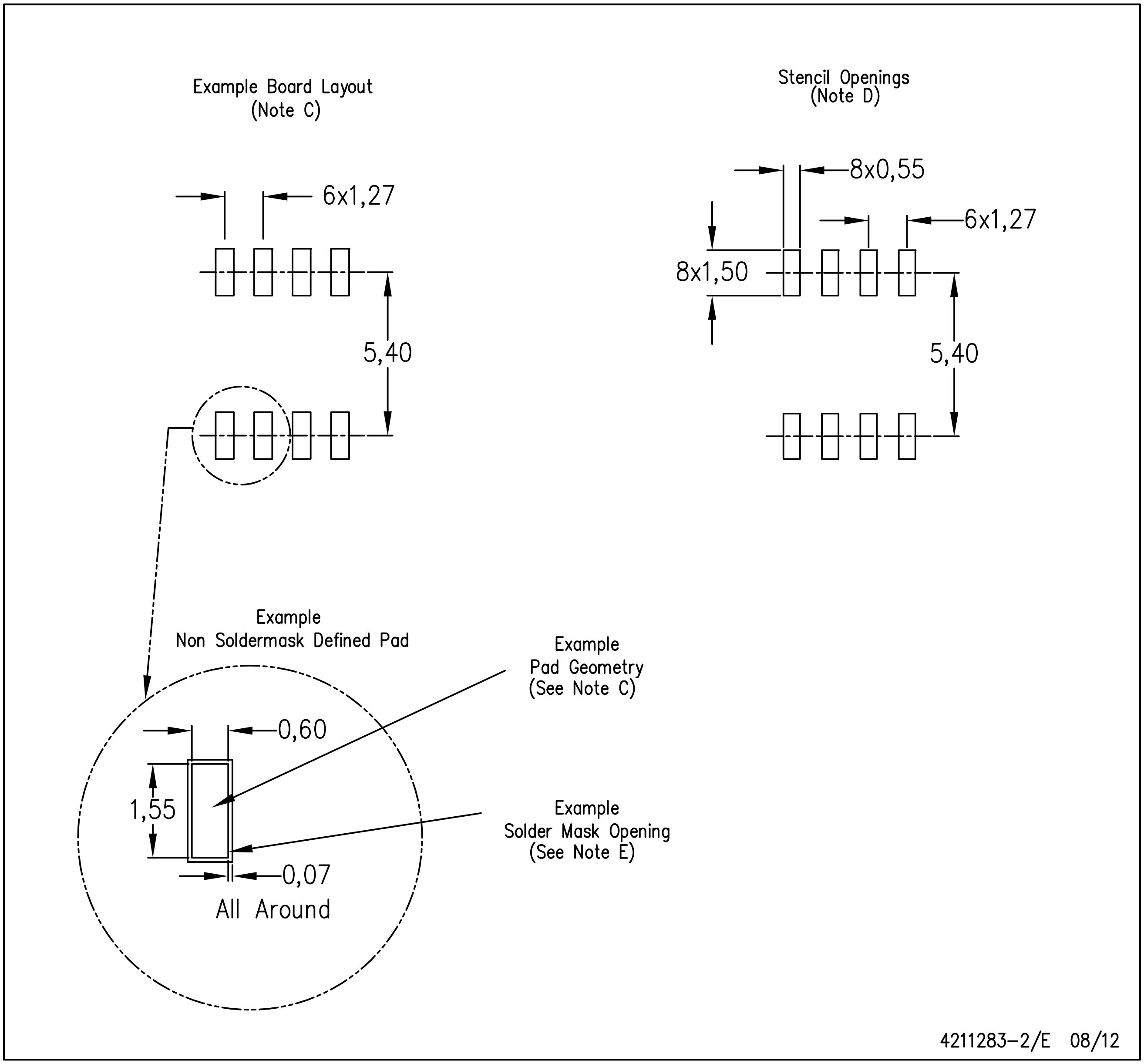
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

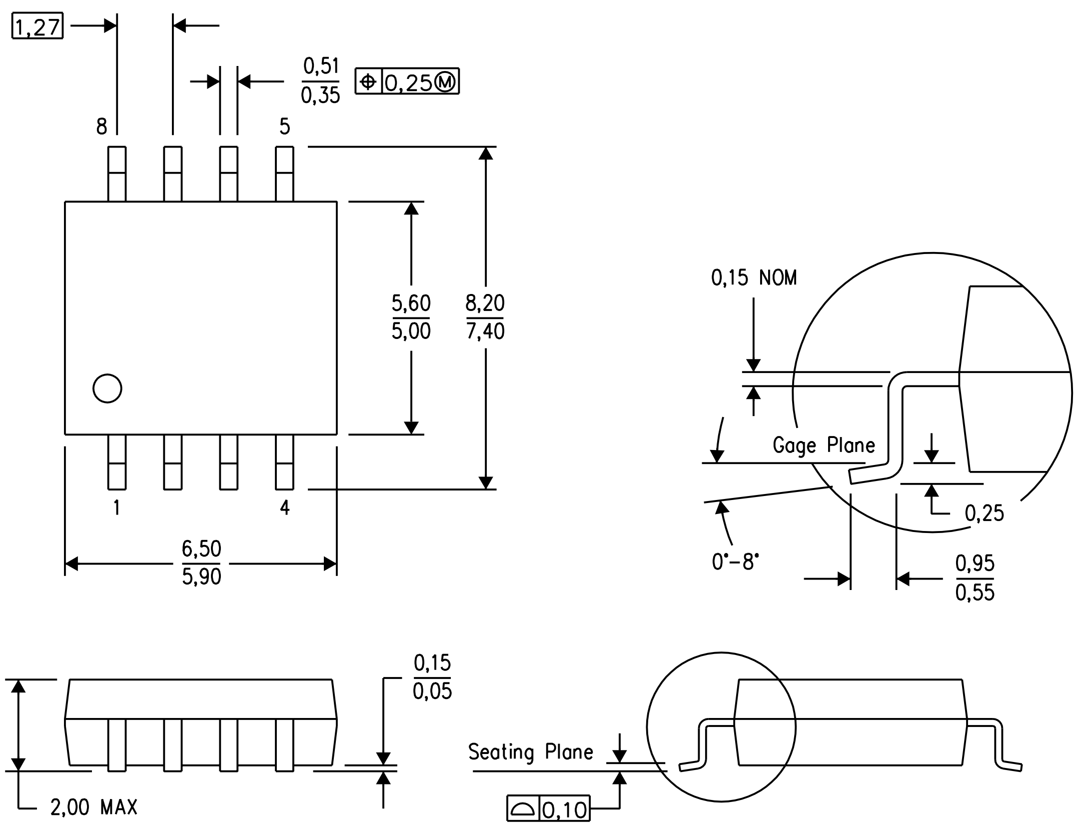
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

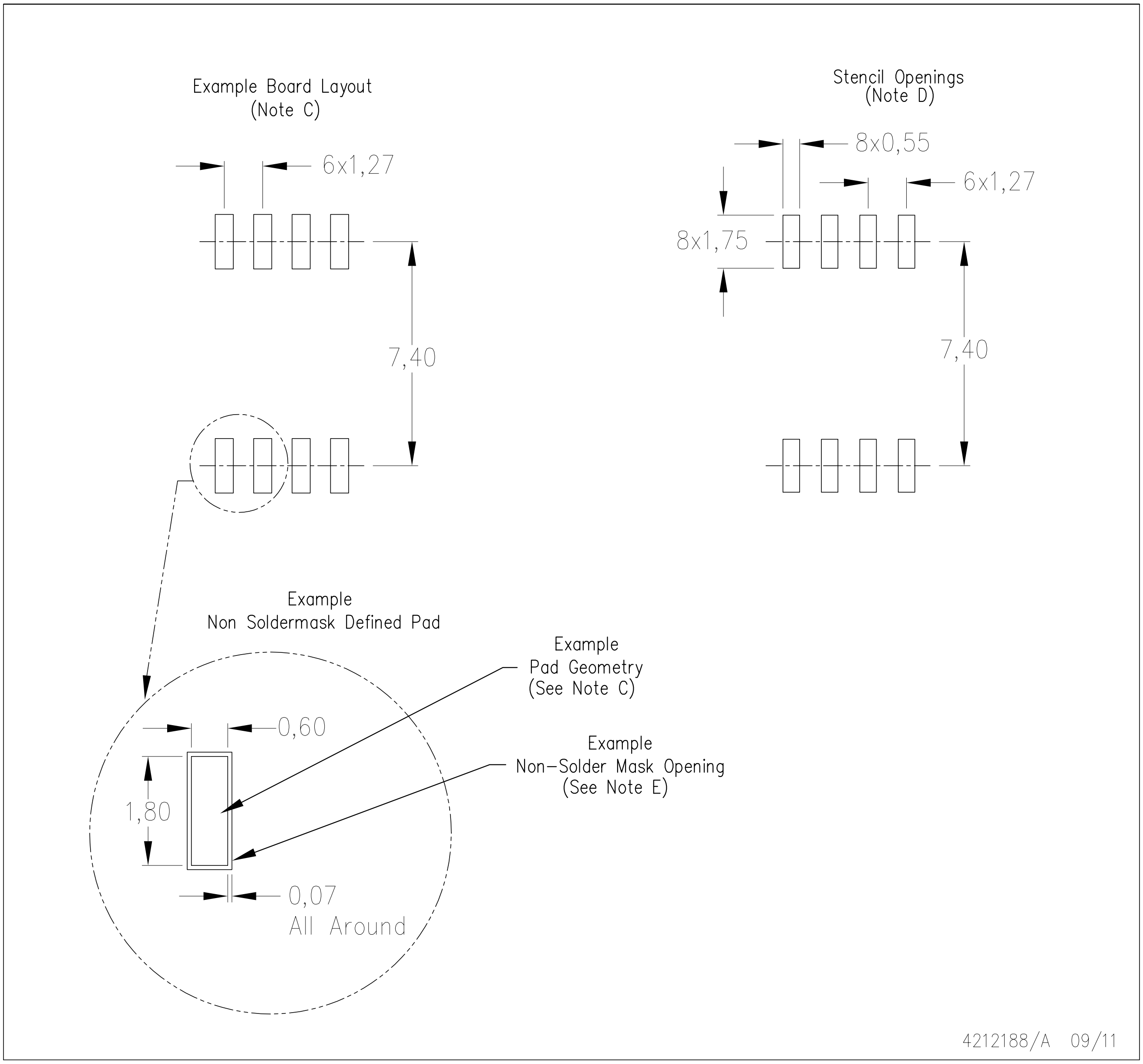
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

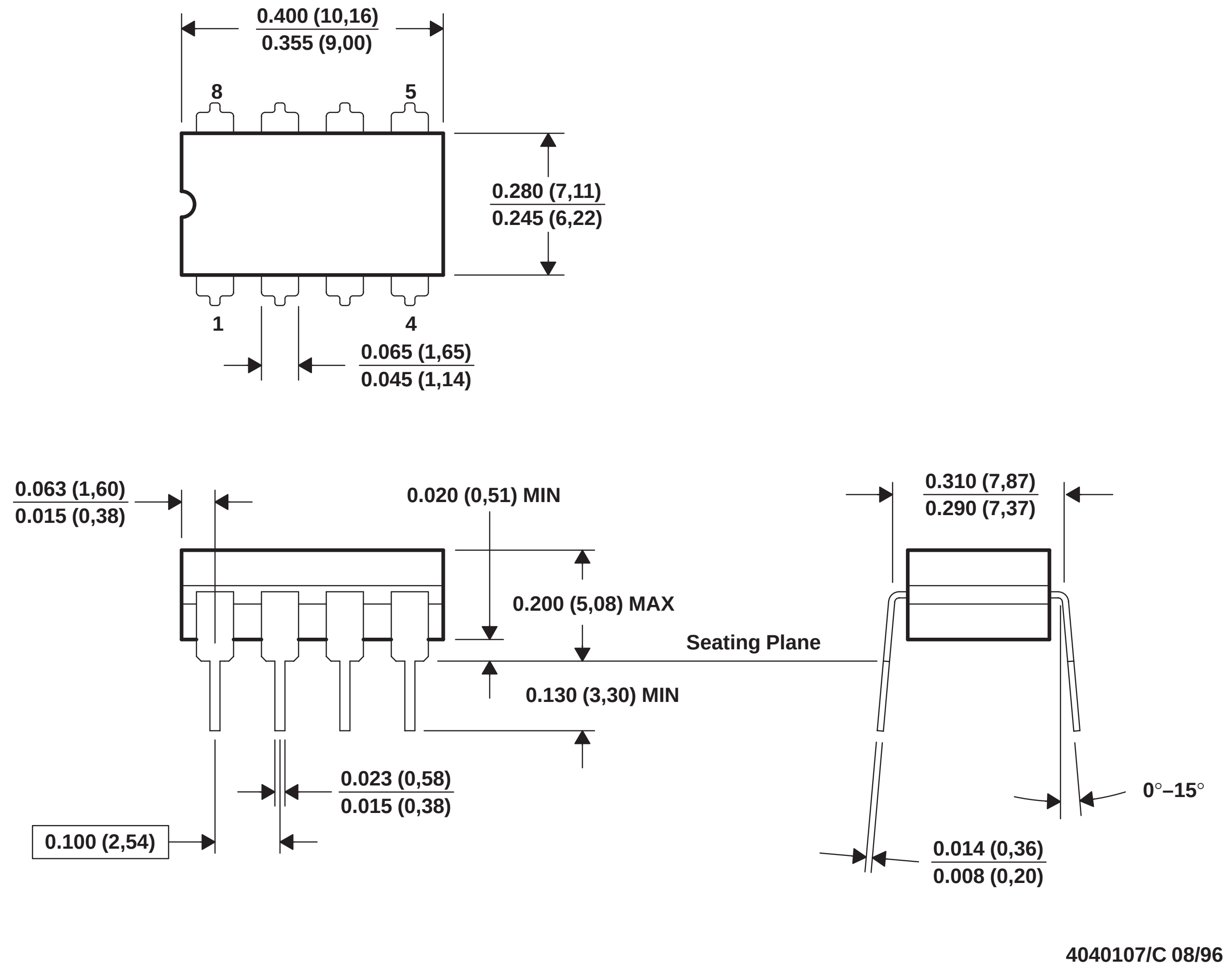
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8) PLASTIC SMALL OUTLINE



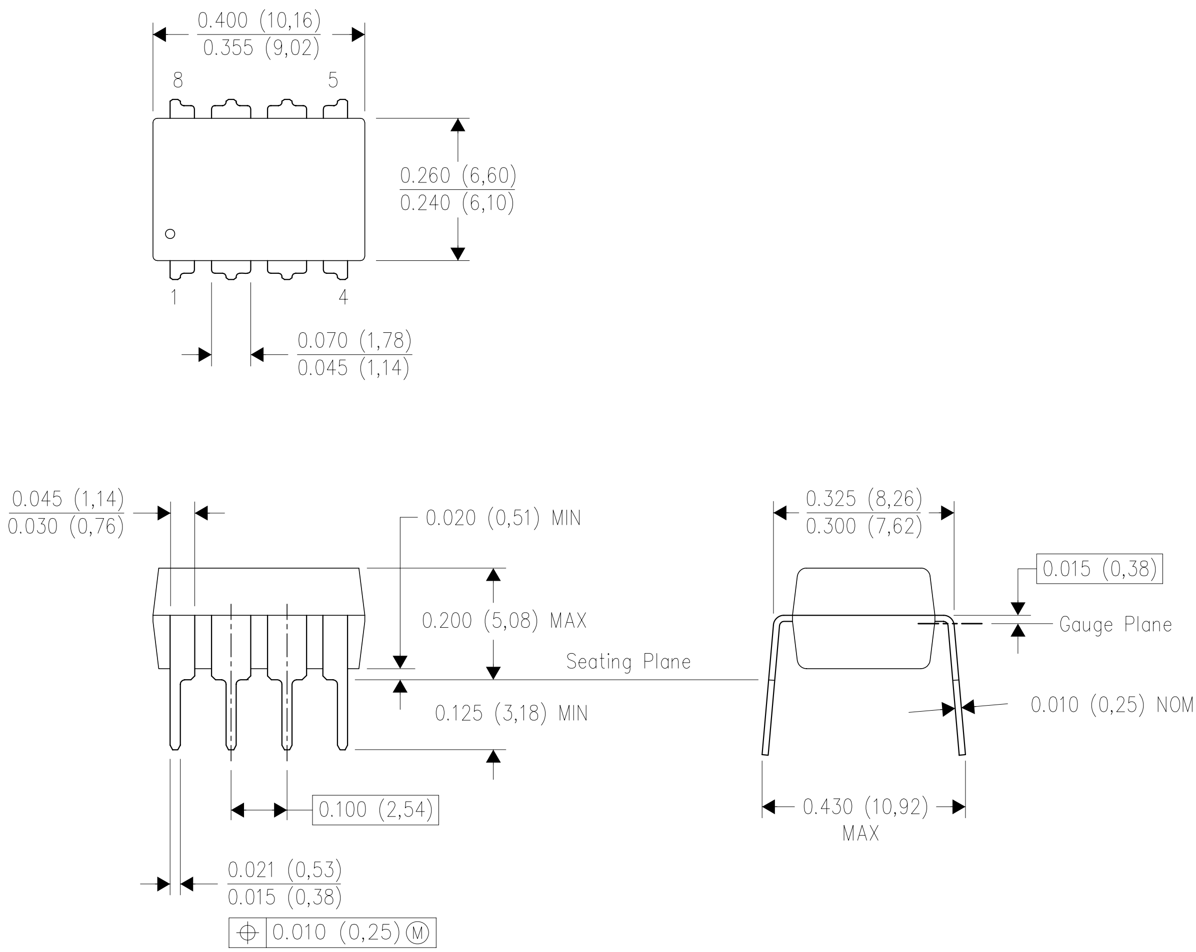
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8) PLASTIC DUAL-IN-LINE PACKAGE

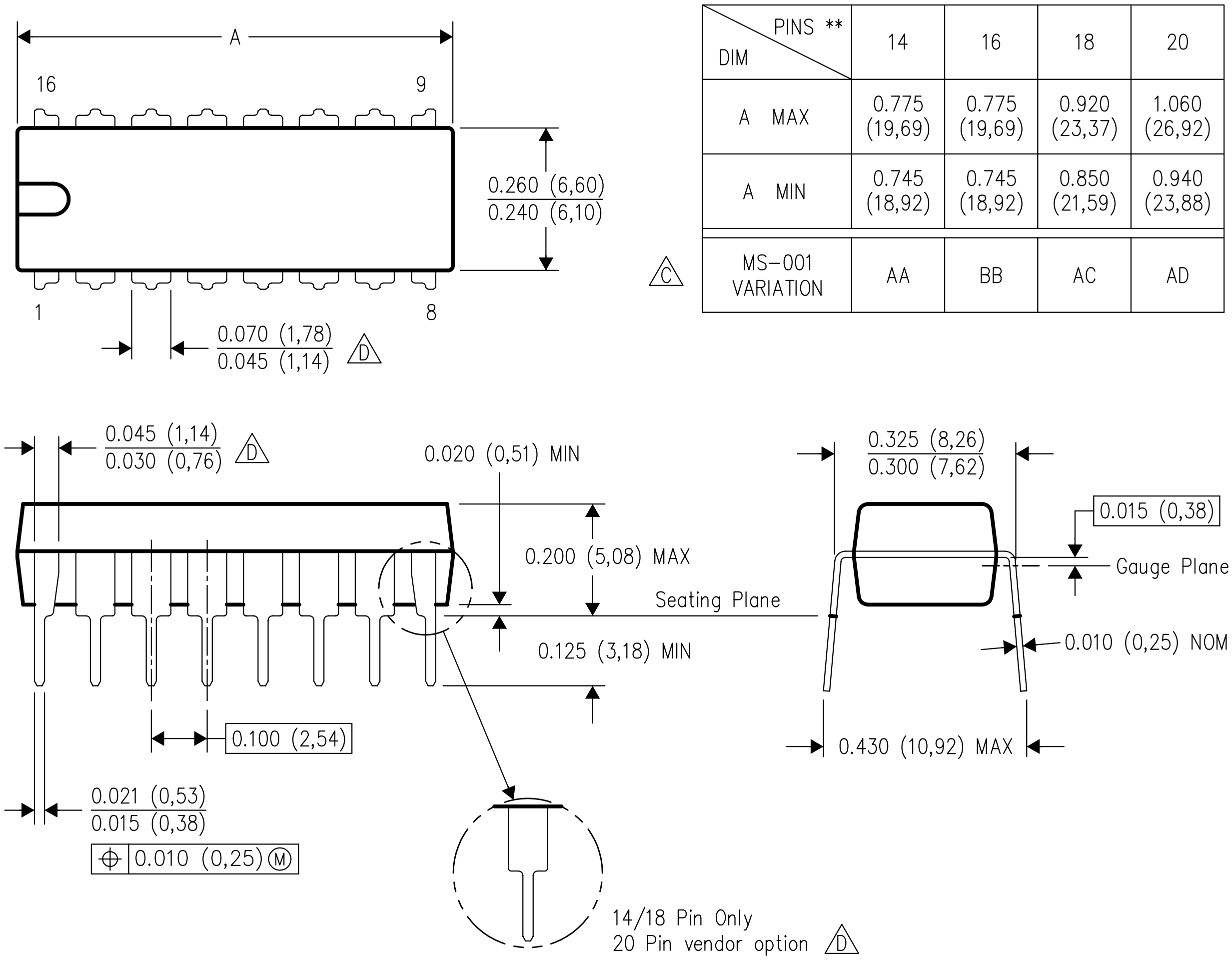


4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

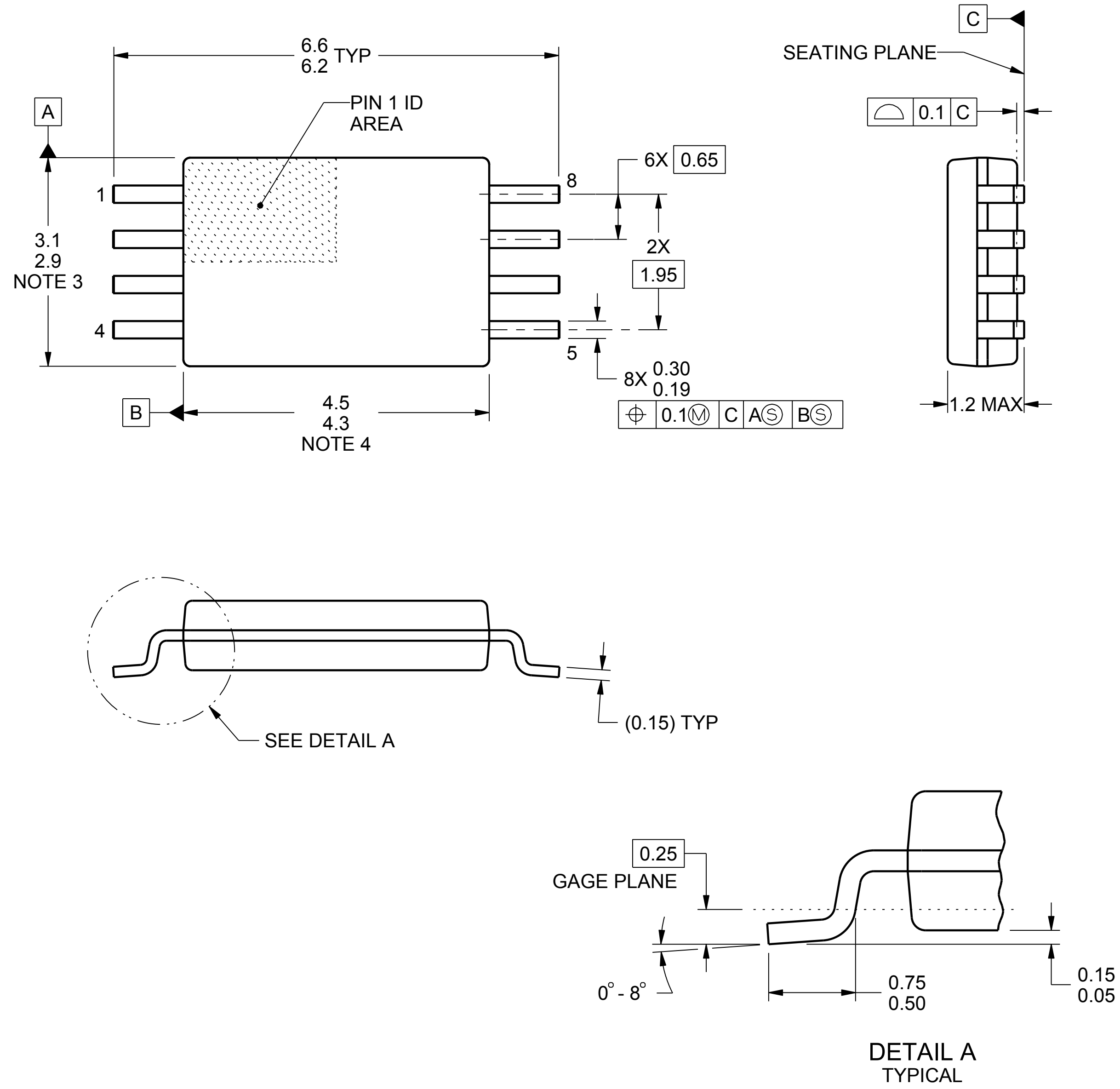
16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

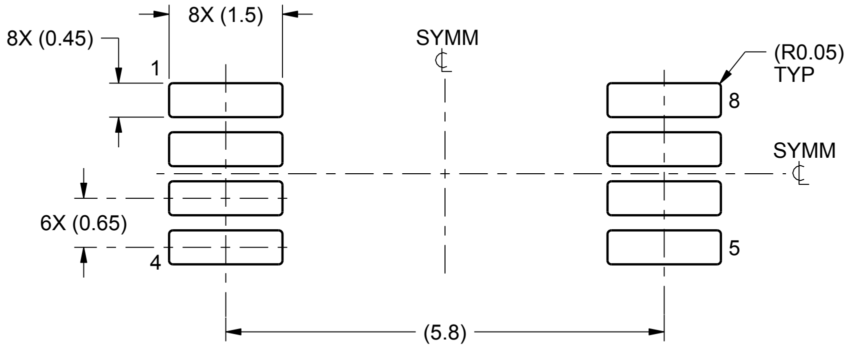
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.



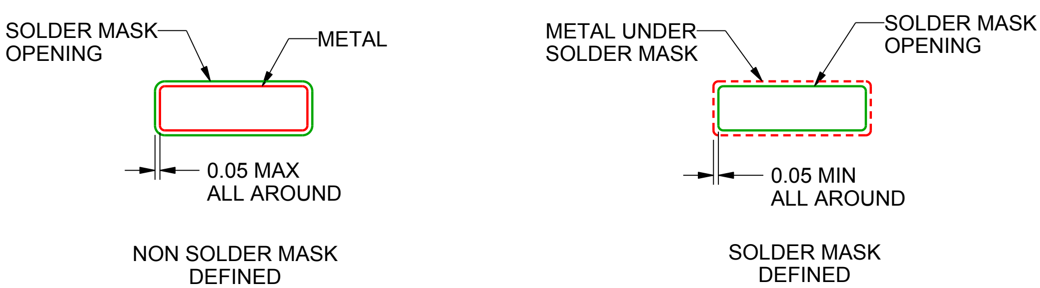
4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

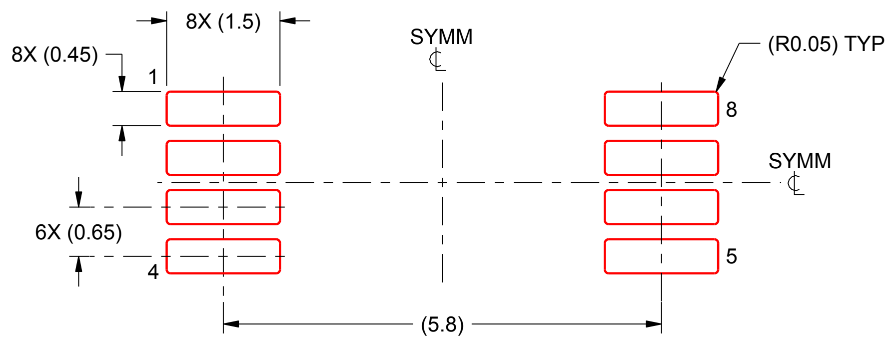


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

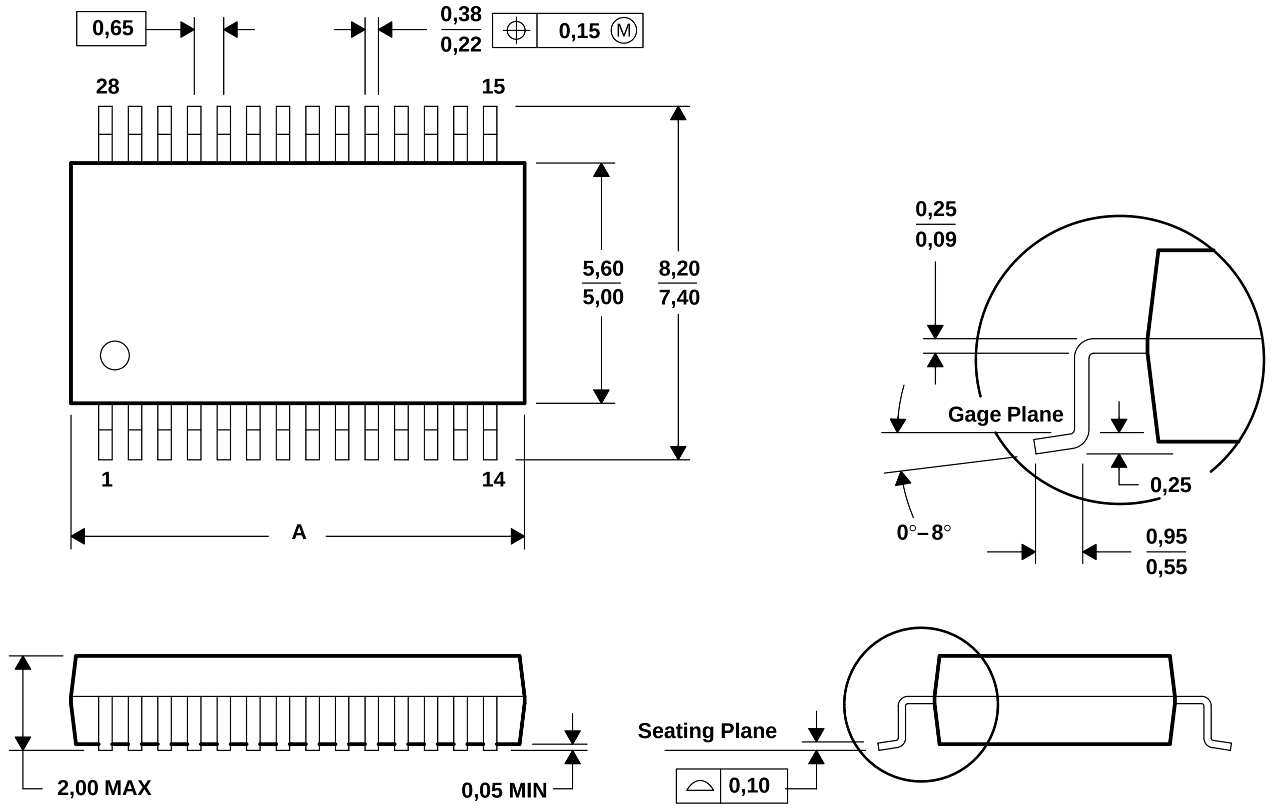
4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

IMPORTANT NOTICE AND DISCLAIMER

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265